GaAs HBTs: An Analog Circuit Design Perspective

John Corcoran, Ken Poulton, and Knud Knudsen

Hewlett-Packard Laboratories
Palo Alto, CA

Abstract

The basic characteristics of GaAs heterojunction bipolar transistors (HBTs) are described, and SPICE parameters of HBT devices are compared to those of a silicon process with breakdown voltage adequate for analog applications. Simulated amplifier bandwidth in the GaAs process is seen to be about twice that of the silicon process at high currents, but the margin decreases at lower currents. Thermal management of HBT IC designs is shown to be important. Simulation tools to control peak junction temperatures and to model thermally induced transients are described.

Introduction

GaAs heterojunction bipolar transistors (HBTs) offer numerous advantages to the circuit designer. These include very high f_T, low collector to substrate capacitance, high output impedance, and good device matching. These properties lend themselves well to the development of very high performance analog circuits, including broadband amplifiers, receiver and transmitter circuits for personal communication ICs, A/D and D/A converters, and a wide variety of microwave circuits. Steady progress in the development of epitaxial materials and IC processes suggests that commercial application may not be too far in the future [1].

In this tutorial paper, we will compare the characteristics of GaAs HBTs to the more familiar silicon devices, with analog circuit applications in mind. SPICE parameters for representative GaAs and silicon devices will be compared, and circuit performance evaluated. Thermal simulation tools for managing GaAs HBT IC design will also be described.

Device Basics

The best measure of performance for a high speed bipolar process is generally f_{max}, the maximum frequency of oscillation for the transistor. f_{max} correlates well in most cases with real circuit performance, such as amplifier bandwidth or logic gate delay, and nearly always is a better figure-of-merit for circuit performance than f_T. But high f_T is still important, since f_{max} is proportional to the geometric mean of f_T and the pole formed by the base resistance R_B and the collector to base capacitance C_{JC} [2]. As one might suspect, there are tradeoffs between optimizing f_T and the R_BC_{JC} pole.

In a traditional silicon (homojunction) device, the emitter must be more heavily doped than the base to maintain good emitter injection efficiency, and thus high beta. For such a device there is a rather direct f_T vs. R_B tradeoff. f_T can be improved by reducing the base transit time with a thinner base region. But making a thinner base increases base resistance, if base doping is held constant by the emitter injection efficiency constraint. So to maintain low R_B with thinner bases, reduced emitter width is required.

In a heterojunction device, the emitter (or base) is made from a material with a different bandgap, which eliminates the constraint that the emitter must be doped more highly than the base [3]. In a GaAs HBT, the emitter is typically made from the wider bandgap material AlGaAs, while the base is made from GaAs. Higher base doping can then be used without degrading emitter injection efficiency. This allows the base to be thinner without sacrificing R_B. The result is a lower base transit time, and an increase in both f_T and f_{max}.

In a GaAs HBT, the base doping is often an order of magnitude higher than in a traditional silicon device, and the emitter doping three orders of magnitude lower. This points out the design freedom allowed by the heterojunction structure. It also leads directly to several other important HBT device characteristics. The very high base doping reduces the effect of collector bias on the base region, i.e. the transistor has a high Early voltage. High base doping also allows low R_B without the submicron geometries typical in silicon devices. Finally, the low emitter doping leads to a low base-emitter depletion capacitance C_{JE}.

Unique Characteristics of GaAs HBT Devices

There are a few ways in which GaAs HBT devices differ from their silicon counterparts, but there are more ways in which they are similar. They are, after all, both bipolar devices, and share the familiar characteristic that collector current is exponentially proportional to qV_{BE}/kT. Therefore all of the circuit designer's knowledge about the basic properties of bipolar transistors, such as gm at a given current, output impedance of emitter followers, the negative temperature coefficient of V_{BE}, etc., will still apply. V_{BE}

matching is good in both technologies, allowing design of precision analog circuits.

It is instructive to plot the common emitter I-V curves of typical GaAs HBT and high speed silicon devices together as in Figs. 1 and 2. (Both devices are specified for operation at a maximum current of about 3 mA.) In Fig. 1, we note the decreasing beta for the GaAs device at low currents. This is typical of GaAs HBTs, where the current gain is usually dominated by recombination effects in the emitter-base space charge region. The GaAs device also shows the high output impedance expected with the higher base doping.

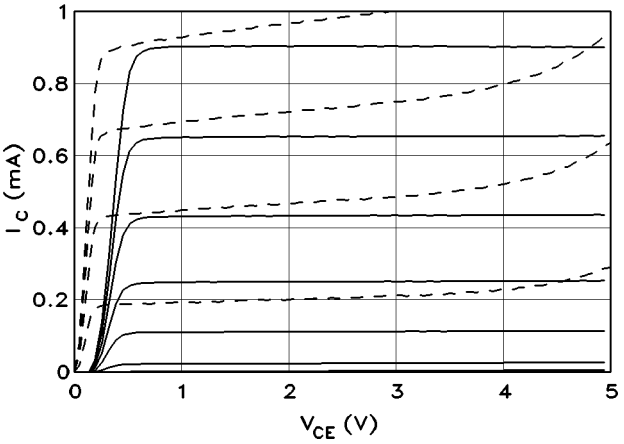

Figure 1: Low current characteristics of 3 mA devices. Solid lines: GaAs HBT; broken lines: silicon bipolar. I_B=2.5 μA/step.

In the high current regime of Fig. 2, we see the GaAs device beta has increased, in this case to beyond that of the silicon device. An interesting feature of Fig. 2 is the negative output impedance of the GaAs device at high currents. This is due to self-heating effects in the transistor, combined with the negative temperature coefficient of beta in GaAs HBTs (of opposite sign to that in silicon). We will have more to say about the circuit implications of temperature effects later.

Among other differences, the V_{BE} of 1.4 V for GaAs HBTs is notable. This necessitates a higher power supply voltage for multi-level amplifiers or ECL circuits. Typically -6 V or -6.5 V supplies are required for 2-level ECL logic, although 2-level CML can operate with standard -5.2 V supplies.

The f_T of GaAs HBTs increases at low V_{CE}, opposite to the trend in silicon. This occurs since the dominant HBT delay is typically across the collector depletion region. This delay drops as the depletion width is reduced.

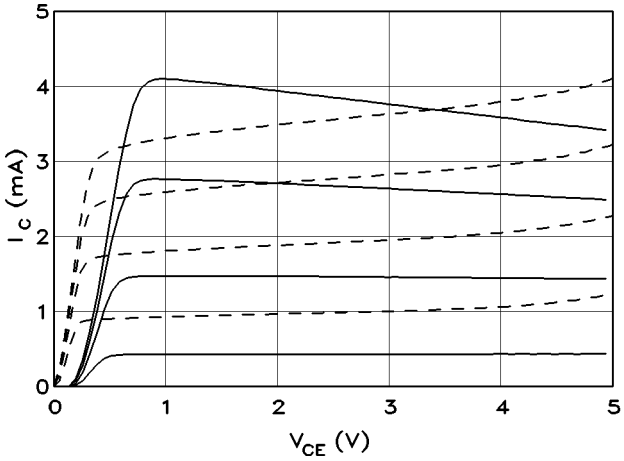

Figure 2: High current characteristics of 3 mA devices. Solid lines: GaAs HBT; broken lines: silicon bipolar. I_B=10 μA/step.

Comparison of Silicon and GaAs Devices

SPICE Parameters

In this section we will attempt to compare SPICE parameters for "state of the art" silicon and GaAs HBT devices. It could be argued that Si-Ge devices represent the state-of-the-art in silicon [4,5]. For our purposes however, they are a bit too state-of-the-art, since as yet (to the authors' knowledge) there have been no complete sets of device parameters published for integrated transistors, nor have there been any circuit demonstrations except ring oscillators [6]. We will therefore compare the two more mature bipolar technologies, GaAs HBTs and conventional (homojunction) silicon devices. This comparison is intended to be a snapshot of the current performance of representative devices, and not a forecast of future device developments.

For the GaAs HBT device, the Rockwell baseline HBT process is a good candidate for comparison. This process is not the highest f_T or f_{max} HBT process reported (even by Rockwell), but key SPICE parameters have been published, and it is not extraordinarily aggressive in the demands it places on the fabrication technology [7]. Furthermore, we have had the opportunity recently to design analog circuits in this process, so it is a convenient choice. This process offers f_T and f_{max} of about 55 GHz, and a breakdown voltage (BV_{CEO}) of 8 V.

How do we choose a silicon process for comparison? For applications in analog circuits, the choice must be qualified on the basis of breakdown voltage. For flex-

ibility in design of high speed analog circuits which handle full scale signals of about 2 V, a BV_{CEO} of 5-6 V is typically required. But there is a fundamental tradeoff between f_T and BV_{CEO} in bipolar devices [8,9]. In simple terms, this tradeoff occurs because higher f_T generally requires higher current density and higher collector doping. The result is a reduction in collector depletion width, and the critical field for avalanche breakdown is reached at a lower collector voltage.

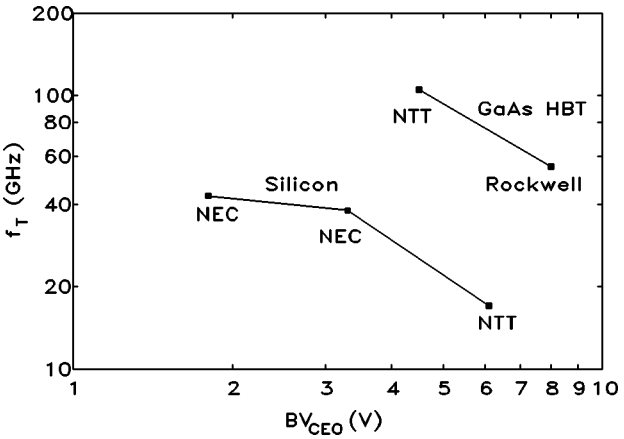

Figure 3: f_T vs. BV_{CEO} for several bipolar processes.

The tradeoff is illustrated in Fig. 3, which plots f_T vs. BV_{CEO} for a few published devices [7,10,11,12]. Both GaAs HBTs and silicon devices are subject to the tradeoff, but we see a higher product of f_T and BV_{CEO} for the GaAs devices, presumably due to their higher mobility and somewhat higher critical field. Although the data plotted here is sparse, the line for silicon indicates that 5 V BV_{CEO} restricts f_T to about 25 GHz. Although there are other important variables in this tradeoff (in particular, beta) we will assert that 25 GHz is a representative silicon f_T for 5 V breakdown. This conclusion is also supported by other published data [6].

The NTT SST silicon process therefore provides a good basis for a comparison. It offers 25 GHz f_T in the SST-1B version [13,14], and a nearly complete set of device characteristics has been published for the SST-1A version [11]. By consolidating the published model parameters and applying some estimated scaling rules, we can make estimates of SPICE parameters for devices of any emitter length, while holding emitter width constant. Due to the liberties thus taken with the NTT parameters, we will describe these devices as simply "the silicon devices", not "the NTT devices". Although the starting point is published NTT parameters, we don't claim that the scaled devices accurately represent real NTT transistors. Likewise, we will generate scaled model parameters for the Rockwell HBT devices, which for simplicity below will be described as "the GaAs devices".

Table 1 contains published device parameters for the silicon [11,13] and GaAs [7,15] devices. For the silicon device, the emitter size is 0.35 x 5 μm^2 and for the GaAs device, 1.4 x 3 μm^2 The silicon device has the narrow emitter stripe required to maintain low R_B at high f_T, as discussed earlier. What conclusions can be drawn from this table? Other than to note that the GaAs device f_T is twice that of the silicon device, practically none, because the rated operating current for these devices has not been specified. A meaningful comparison for high speed applications can only be done between devices specified to operate at the *same current.* For the GaAs device, the maximum operating current is specified at 0.8 mA/μm^2 of emitter area [15]. Coincidentally, we find peak f_T very close to 0.8 mA/μm^2 for the silicon process also [13]. So equal maximum current densities will be assumed. To compare devices specified for operation at the same current, the emitter areas must therefore be made equal.

	GaAs Device	Silicon Device
Emitter size	1.4 x 3 μm^2	0.35 x 5 μm^2
f_T	55 GHz	25 GHz
C_{JC}	11 fF	7.4 fF
C_{JE}	7 fF	10.4 fF
C_{JS}	3 fF	22.9 fF
R_B	110 Ω	310 Ω
R_E	15 Ω	18.5 Ω

Table 1. SPICE parameters for published GaAs HBT and silicon devices.

Table 2 shows device parameters for the same emitter areas, i.e an emitter of 0.35 x 12 μm^2 for the silicon device, and 1.4 x 3 μm^2 for the GaAs device. Each of these devices would be rated at 3.4 mA. (For the silicon device, a linear scaling was done for C_{JE}, R_B, and R_E, and a slower than linear scaling for C_{JC} and C_{JS}.) Table 2 shows a large advantage for the HBT device in f_T, C_{JE}, and C_{JS}. The advantage in C_{JE} is expected for the same emitter area, due to the much lower doping in the HBT emitter. The C_{JS} (collector to substrate capacitance) advantage follows from the semi-insulating GaAs substrate. The advantage in C_{JC} is seen to be smaller (about 30%), and the base resistances are about equal. The silicon device shows a 2X advantage in emitter resistance.

Although it is important to compare parameters for devices specified to operate at the same current as above, a minimum emitter length would normally be chosen by the circuit designer for very low current applications. Table 3 therefore shows projected device parameters for emitter lengths of 2 microns, an assumed reasonable minimum for both technologies. Due to the large scaling factor applied to the silicon device relative to Table 2 (from 12 μm to 2 μm), C_{JC} is now less than half that in the GaAs HBT, and C_{JE} is about equal. But the silicon device shows an R_B five times and an R_E two times that of the GaAs device.

	GaAs Device	Silicon Device
Emitter size	1.4 x 3 μm^2	0.35 x 12 μm^2
Max current	3.4 mA	3.4 mA
f_T	55 GHz	25 GHz
C_{JC}	11 fF	16 fF
C_{JE}	7 fF	25 fF
C_{JS}	3 fF	41 fF
R_B	110 Ω	129 Ω
R_E	15 Ω	7.5 Ω

Table 2. SPICE parameters for GaAs and silicon devices. The silicon device has been scaled in size to give the same maximum current as the GaAs device.

	GaAs Device	Silicon Device
Emitter size	1.4 x 2 μm^2	0.35 x 2 μm^2
Max current	2.3 mA	0.6 mA
f_T	~55 GHz	~25 GHz
C_{JC}	8.8 fF	3.7 fF
C_{JE}	4.8 fF	4.2 fF
C_{JS}	3 fF	15 fF
R_B	149 Ω	775 Ω
R_E	22 Ω	45 Ω

Table 3. SPICE parameters generated by scaling to minimum emitter length, assumed to be 2 microns.

Broadband Amplifier Example

It is difficult by inspection to assess the impact of the parameter differences in Tables 2 and 3, so SPICE simulation was used on a simple analog circuit, the emitter degenerated differential amplifier of Fig. 4. The objective of this exercise was to find the bandwidth of the circuit vs. bias current of the transistors, and to assess the impact of emitter length scaling on bandwidth. Three circuits of this type were cascaded (to provide reasonable driving point and termination impedances) and the bandwidth of the second stage was recorded.

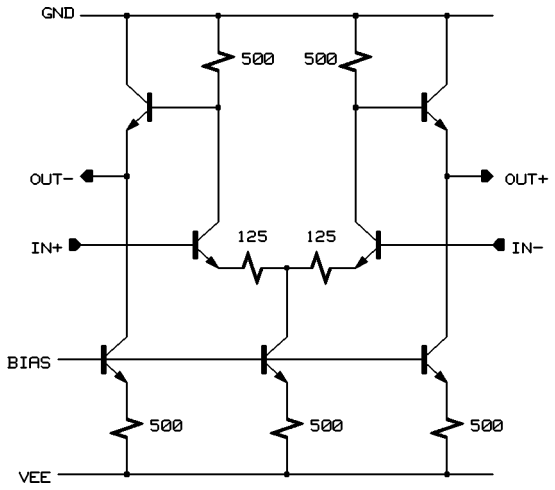

Figure 4: Broadband amplifier example. Resistor values (shown for 1 mA case) scale inversely with current. Transistor scaling is described in the text.

First, the transistor sizes in Fig. 3 were fixed at 1.4 x 3 μm^2 for the GaAs device and 0.35 x 12 μm^2 for the silicon device, corresponding to the device parameters in Table 2. The bias current for each transistor was then set at each of several currents, up to the allowed maximum of 3.4 mA. The resistor values were scaled inversely with current, and after small additional adjustments to the collector load resistors to set the gain to a constant 10 dB, the bandwidth was recorded.

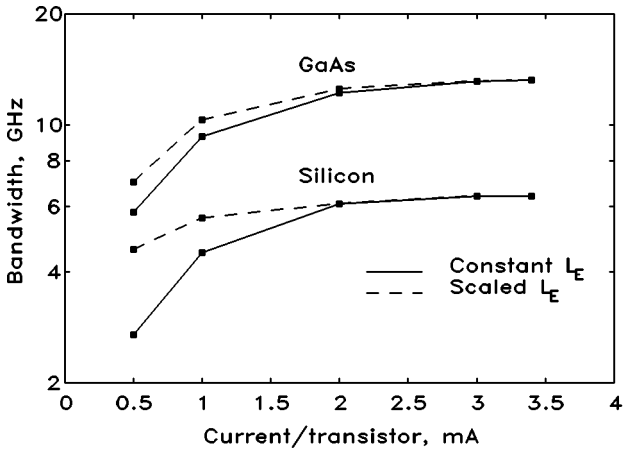

Figure 5: Simulated amplifier bandwidths vs. current per transistor.

Next, the transistor sizes were scaled as the currents were varied, in each case using the smallest transistor allowed without exceeding the current rating of 0.8

mA/μm^2. For the silicon devices, this meant scaling the emitter length from 12 to 2 μm, and for the GaAs device, from 3 to 2 μm.

The results are shown in Fig. 5. For constant emitter length, the GaAs amplifier has a bandwidth very close to twice that of the silicon device over the entire bias current range. This advantage is expected, since both f_T and the $R_B C_{JC}$ pole are significantly higher in the GaAs models of Table 2. When emitter length is scaled with current, the advantage in the GaAs case drops to about 1.5X at 0.5 mA, presumably due to the higher scalability of the narrow-emitter silicon device.

To learn which device parameters were responsible for the reduced bandwidth ratio at low currents, a sensitivity analysis was performed. The results are shown in Table 4. For the GaAs circuit, the bandwidth is almost completely controlled by C_{JC}. For the silicon case, C_{JS} and C_{JC} are both important, but at a lower sensitivity than in the GaAs case. It is interesting to note that the higher R_B and R_E in the silicon case do not result in high sensitivities, presumably because the resistors in the circuit also have been scaled up for low current operation.

Parameter	GaAs Amp	Silicon Amp
τ_f	0.07	0.20
C_{JC}	0.75	0.33
C_{JE}	0.03	0.02
C_{JS}	0.06	0.35
R_B	0.08	0.13
R_E	0.01	0.01

Table 4. Sensitivity factors for amplifier bandwidth at 0.5 mA operating current and L_E=2 μm. Sensitivity is percent change in bandwidth divided by percent change in parameter.

From this exercise, one can conclude that C_{JC} reduction is a high leverage parameter for improvements in HBT amplifier bandwidth at low currents. It should be pointed out that a damage implant under the extrinsic base has been used as a way to obtain C_{JC} reduction in HBTs [16]. The SPICE parameters used in this study did not reflect use of such an implant.

Microwave Applications

The semi-insulating GaAs substrate makes HBT devices considerably better suited than silicon to microwave applications. The advantage follows from the low loss properties of the substrate, which allows high quality on-chip transmission lines and inductors. Likewise, large area structures like bonding pads and coupling capacitors can be formed with quite low parasitic capacitance to ground. GaAs HBTs can be expected to compete effectively with GaAs FETs in the microwave market, offering many of the same advantages and perhaps improved performance in some areas like 1/f noise, important for low phase noise oscillators.

Mixed microwave-digital applications (for example, integrated tuners with phase locked oscillators) also look quite promising, since low power logic functions can be implemented more efficiently than in the high I_{DSS} depletion mode processes typically used for GaAs FET microwave circuits.

Data Acquisition Applications

GaAs HBTs show considerable promise for data acquisition applications, like A/D and D/A converters and sample and hold circuits. For these applications, an important device figure-of-merit is the standard deviation (sigma) of differential pair offset voltage. For a Rockwell GaAs HBT an offset voltage sigma of 1.3 mV has been measured in the lab [15] for a 1.4 x 3 μm^2 emitter at 1 mA bias current. This is adequate for 6 to 8-bit parallel ("flash") type A/D converters.

Emitter area matching is clearly important for low offset voltage. HBTs may have an edge in this regard due to the typically larger emitter width. One reported A/D [18] designed in the NTT SST-1B process used a 1 μm emitter width in the preamp devices to improve matching, presumably at the expense of higher R_B.

But emitter resistance is also important, since it can degrade matching as current is increased. The silicon device in our comparison above had an emitter resistance (per unit area) one half that of the GaAs device, which would predict better matching for silicon at higher currents.

A/D converters include a substantial amount of logic, so gate delays and power-delay product are of interest. Simulated ECL gate delays (fanout=1) are 15 ps at 1 mA bias currents for the GaAs HBT devices used in the technology comparison above. Likewise, for the silicon process, simulation predicts 33 ps delays under the same conditions, including scaling for optimum emitter length. This agrees well with the measured delay of 34 ps reported for the NTT SST-1B process [13], from which the silicon device models were derived.

For sample and hold circuits, fast Schottky diodes are an important building block. The product of diode on-resistance and zero-biased capacitance is often used as figure-of-merit. For GaAs HBTs, this product can be less than 0.5 ps, and is expected to be

considerably better than that obtained in silicon due to the higher electron mobility in GaAs. The lack of a significant capacitance to the substrate is also an advantage for GaAs Schottky diodes.

Thermal Properties of GaAs HBTs

Control of Junction Temperatures

Unless the circuit designer and IC layout designer are aware of the thermal properties of GaAs HBTs, problems with excessive operating temperatures can arise. This is partly due to the high current density associated with high f_T, which is a property common to both silicon and GaAs devices. But two other factors contribute to higher GaAs HBT junction temperatures: The thermal resistivity of GaAs is about three times that of silicon, so three times higher thermal resistance is expected for devices of the same geometry; and the relatively wide, short emitters typically used in HBTs have a higher thermal resistance than the narrow, long emitters required in silicon. For example, three-dimensional thermal simulation predicts about a 6X lower thermal resistance for a 0.35 x 12 μm^2 dissipation region in silicon than for one which is 1.4 x 3 μm^2 in GaAs. That is, there is a 2X effect due to this geometry difference.

In a closely packed layout, the effect of "proximity heating" is also important. That is, each transistor heats its neighbors, and the absolute junction temperatures will be higher than those predicted from self-heating alone. Since modern silicon and GaAs HBT devices are quite small compared to the thickness of the substrate (which approximates the effective range of proximity heating), this effect can be quite large. Assuming the same power density, we would expect the amount of proximity heating to scale with the thermal resistance of the substrate, suggesting a three times higher effect in GaAs.

We have carried out three-dimensional finite-difference simulations to compute thermal resistances of specific GaAs HBT devices. For a 1.4 x 3 μm^2 device, a thermal resistance of 2.7 °C/mW is predicted. This value agrees well with junction temperatures inferred from the change in beta with power dissipation in actual device measurements, although less perfect agreement was found for larger device sizes [19].

Armed with knowledge of device thermal resistances, but without a method of computing proximity heating effects, we designed and laid out an HBT sample and hold circuit. The thermal design objective was to keep self-heating temperature rises below 40 °C. The resulting circuit suffered from severe overheating problems and short device lifetimes, since proximity heating had not been modeled.

As a result of this experience, a fast whole-chip thermal simulator was developed [20]. Inputs to the simulator are the locations, sizes and powers of all power dissipating elements in the circuit. The geometrical information is transferred from the layout data base; the power dissipation in each of the elements is obtained from the text file of a SPICE simulation. The output of the simulator is a listing of hottest devices, or a thermal contour plot of the chip.

Fig. 6 is a simulated thermal contour plot for the sample and hold chip described above. The contour lines are densest, and the predicted temperatures highest, near the very high performance sampler circuit. Although it can't be read from the contour plot, the predicted rise of the hottest HBT was 255 °C, meaning that a 215 °C rise was apparently occurring due to proximity heating effects. It should be pointed out that this simulation was for a 25 mil wafer thickness and an epoxy die attach.

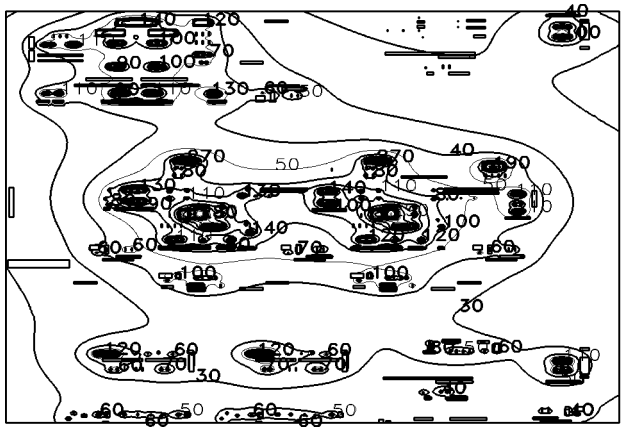

Figure 6: Simulated thermal contour plot of an HBT sample and hold chip. Numbers are temperature rise in °C.

This sample and hold circuit was then laid out again, using the thermal simulator as a guide to control proximity heating. Predicted rise to the hottest HBT was reduced to 154 °C with only a 25% increase in area of the layout. Assuming backlapping of the wafer to 3 mils before packaging (to reduce the range of proximity heating) and using a soldered die attach, the simulator predicts an acceptable peak rise of 71 °C.

The new layout has been fabricated and there are no signs of thermal problems or short device lifetimes. Although the absolute accuracy of the thermal simulator is still in the verification process, we believe that

the use of such tools will be required to successfully manage dense, high current layouts of analog HBT ICs. Present silicon processes might also benefit from the use of thermal simulation. Future processes will likely require it if they operate at significantly higher current densities.

Thermally Induced Transients

Thermal transients are a known phenomenon in high current bipolar analog circuits. A typical example is a dc-coupled amplifier whose step response initially includes an overshoot or undershoot, which then relaxes with thermally related time constants. In general, these effects are most important in dc coupled circuits where step response is important, such as amplifiers or A/D converters for waveform capture applications. But they may also be important in some ac-coupled circuits requiring high gain flatness with frequency.

Not surprisingly, these phenomena also occur in GaAs HBTs, and due to higher device thermal resistances can be expected to be larger than in silicon. To model these effects, we built a thermal subcircuit in SPICE, which adds a controlled voltage source in the base lead and a controlled current source across the base emitter junction of each transistor. These are used to model two thermal effects in the transistor, the negative coefficients of V_{BE} and beta with temperature. Temperature is calculated in SPICE from the power dissipation of the device and the assumed thermal resistance, and used to vary the controlled sources.

This model provides a much better match to the I-V characteristics of the transistor than the simple SPICE BJT model. Fig. 7 shows the I-V curves for a 1.4 x 3 μm^2 HBT device, with the thermal SPICE curves added. The negative slope in the high current regime (due to temperature effects) is reproduced well by the model.

Another feature of the model is that the power dissipation computed in SPICE is converted to a current and applied to a cascade of RC filters, which model the distributed thermal resistance and capacitance of the device. The resulting voltage gives the temperature of the device as a function of time, and is used to vary the controlled sources described above. This allows AC and transient simulations with correct frequency behavior.

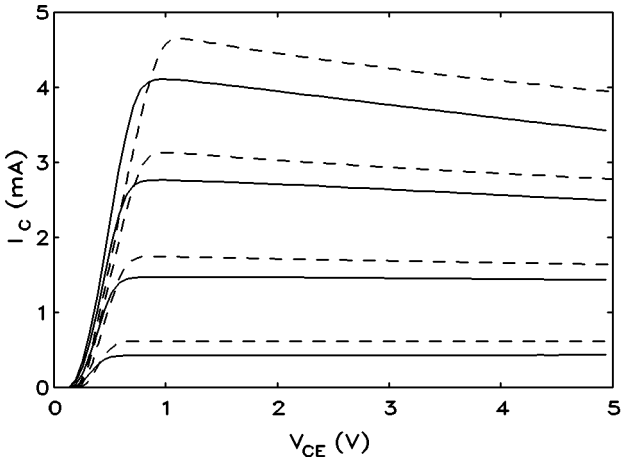

Figure 7: Measured (solid line) and simulated (broken line) I-V characteristic of a GaAs HBT, using a thermal model in SPICE; I_B = 10 μA/step.

To test the correctness of the model we measured the gain of an emitter follower vs. frequency with an HP 3577 network analyzer. The device tested was a 1.4 x 3 μm^2 HBT, loaded by a 10 KΩ resistor as a current source. The thermal effect occurs in the following fashion: When the input signal to the follower rises, the transistor's power dissipation decreases due to lower V_{CE}. The temperature coefficient of V_{BE} then causes the output of the follower to fall slightly as the device temperature drops. Since the effect is proportional to the amount of the input change, there is a gain reduction at low frequency, where the thermal effect occurs. (In the time domain this would be manifested as an overshoot in the step response).

Fig. 8 shows the measured and simulated results for the emitter follower gain at two different bias currents. Both measurement and simulation show the gain reduction at low frequency, which then begins to diminish at around 100 kHz. The simulation shows the thermal effects don't completely disappear until about 100 MHz. Due to probe card bandwidth limits, the measured gain rolls off before this frequency is reached.

The magnitude of the gain depression observed at low frequency is about 0.09 dB (1.0%) at 3.4 mA bias. Although this is relatively small, it will be higher for larger transistors run at the same current density, because thermal resistance does not decrease linearly with increasing device size. It of course will also be correspondingly larger for cascaded amplifier stages. However, these effects can be controlled by various circuit techniques; for the emitter follower above, bootstrapping of the collector to the base would essentially eliminate the effect.

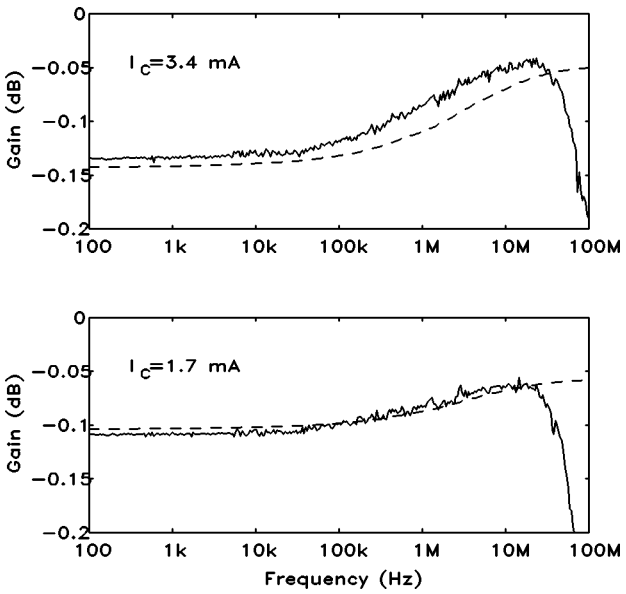

Figure 8: Measured and simulated gain of an emitter folllower showing thermal gain changes. Bandwidth of the measured response is limited by the probe card.

Summary

Analog circuit design techniques for GaAs HBTs are similar to those used with silicon devices, but the larger V_{BE} and the increased need to monitor the thermal characteristics of the design in GaAs are important differences. Compared to a representative silicon process qualified on the basis of breakdown voltage, GaAs HBT devices have been shown to offer about twice the bandwidth in a simple differential amplifier biased for operation near peak f_T. The increased scalability of the silicon device reduces this advantage at low currents.

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