Interleaved ADCs Through the Ages

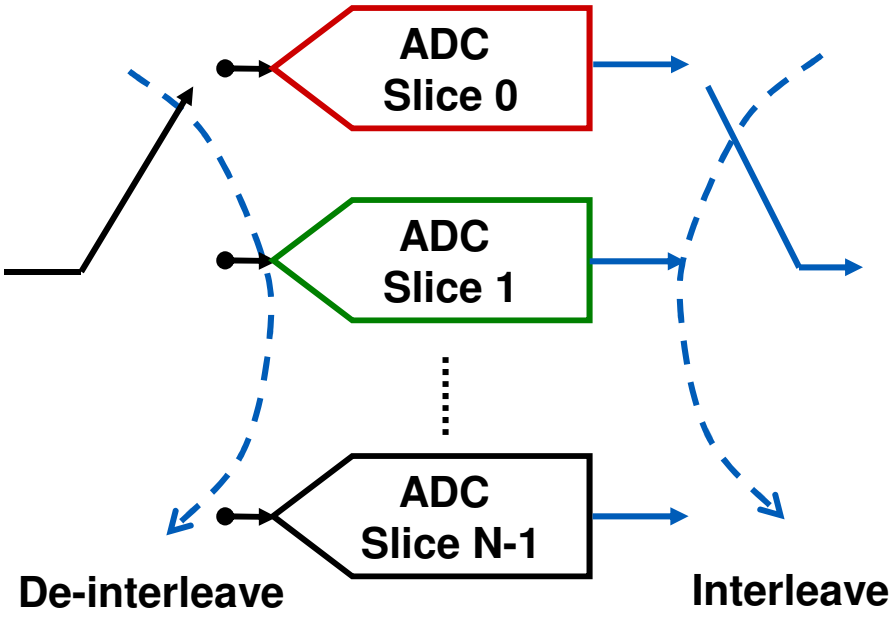
Ken Poulton
Keysight Laboratories

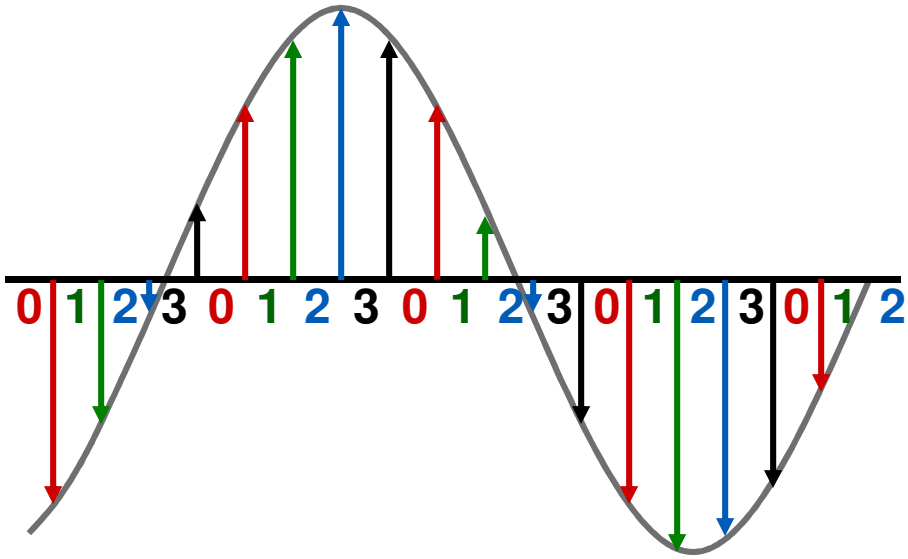
Topics

- What is Time Interleaving
- History of Time Interleaving
- ADCs for Oscilloscopes (and Other Instruments)
- Frequency Interleaving
- Issues in Interleaved ADCs and Some Solutions

But not really in that order…

Time Interleaving Idea





- Unit (slice) ADC speed is limited by comparator and amplifier speed
- Interleave multiple ADC slices to increase total sampling rate

Reasons for Time Interleaving

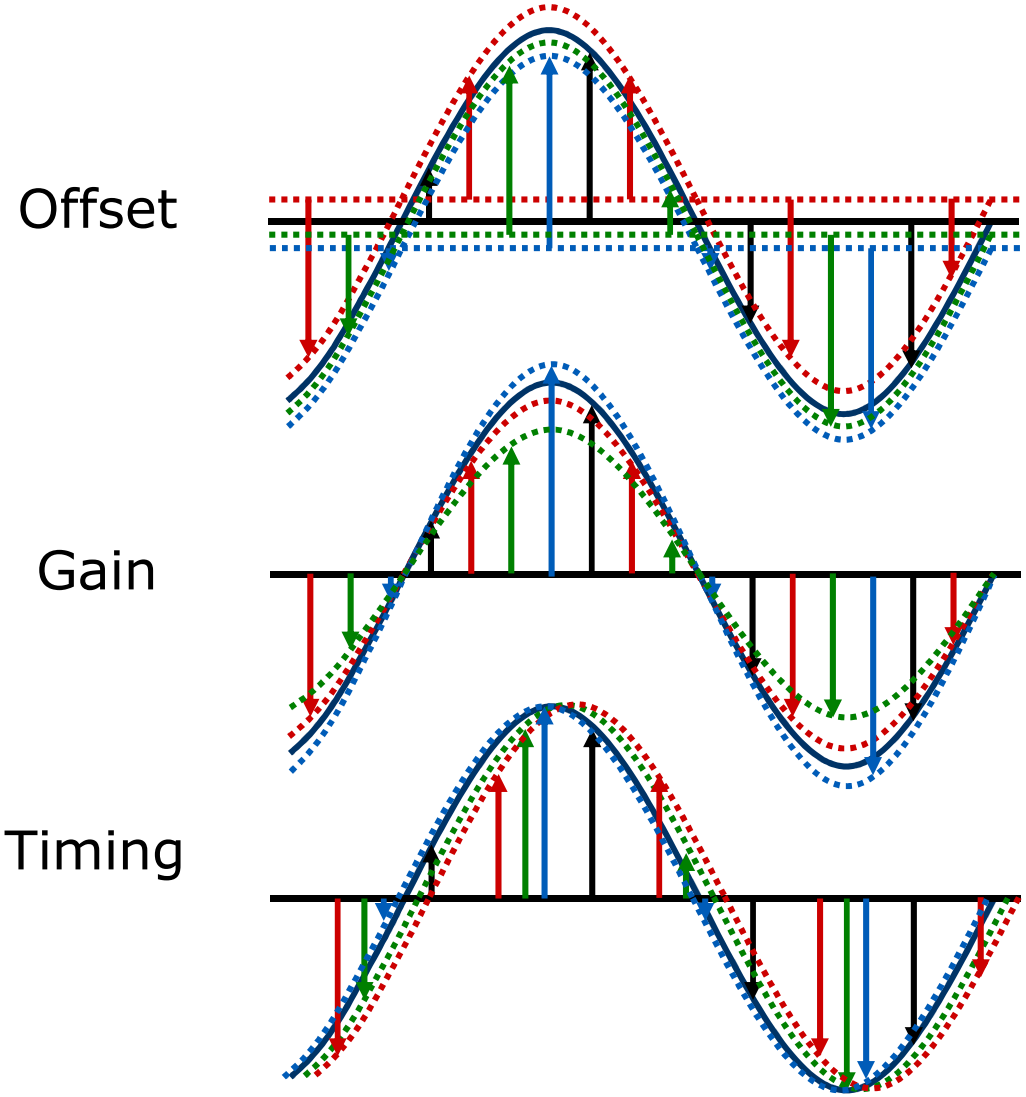
- Speed
  - Sample rate multiplied by N_{slices}
  - Nyquist BW multiplied by N_{slices}
- Power Efficiency
  - The ADC slice can operate at its most *efficient* sample rate
- Process choice
  - Can use a slower process for a given total sample rate

Issues with Time Interleaving

- Analog Bandwidth goes *down*
  - Many slices connected to the analog input
- Interleaving errors due to slice-to-slice mismatch
- Complexity
  - N times as much ADC hardware
  - Additional clock generation, much of it critical
  - Additional circuits to improve the BW and interleaving errors

Types of Interleaving Errors

Due to Slice-to-Slice Mismatch



Results of Interleaving Errors

Error Type
(and size for 8 bits)

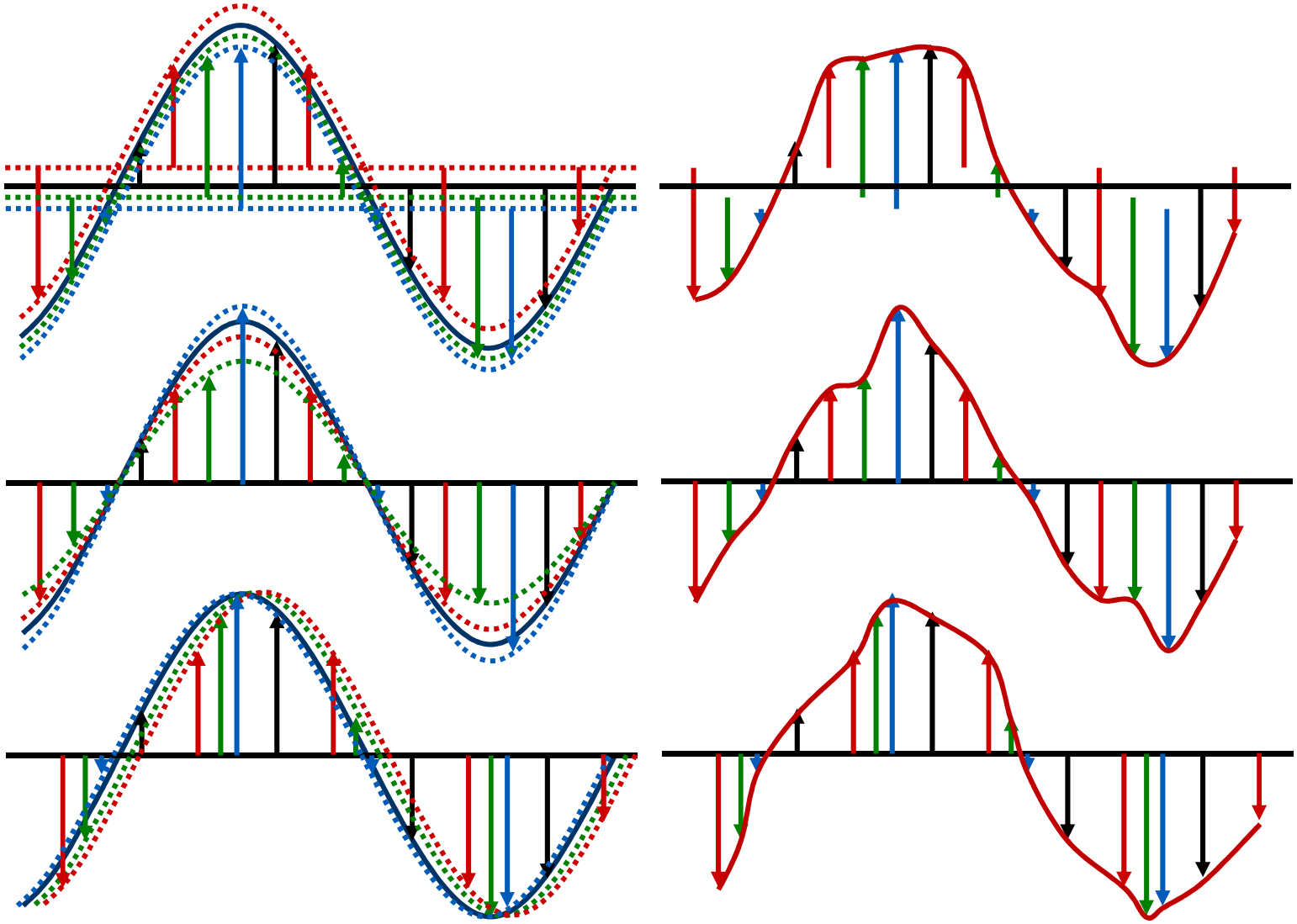
Slice Waveforms

Reconstructed Waveform

Offset
<0.3%

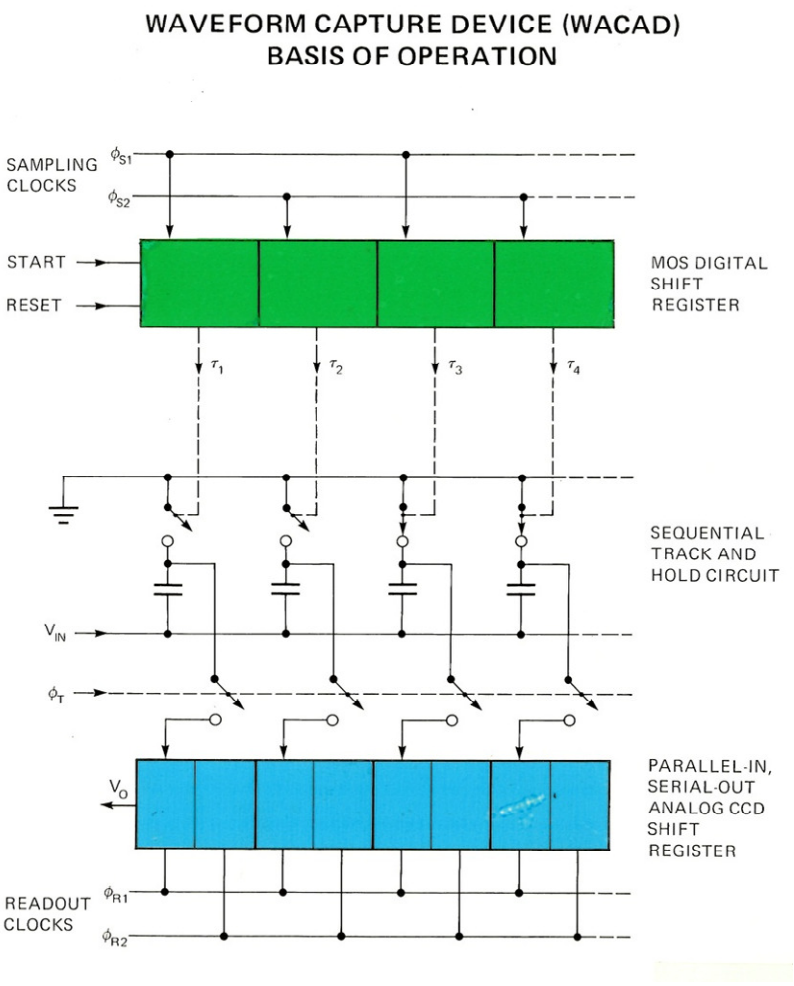
Gain
< 0.3%

Timing
< 0.5 ps for Fin = 1 GHz



1980: First Interleaving - Analog Storage

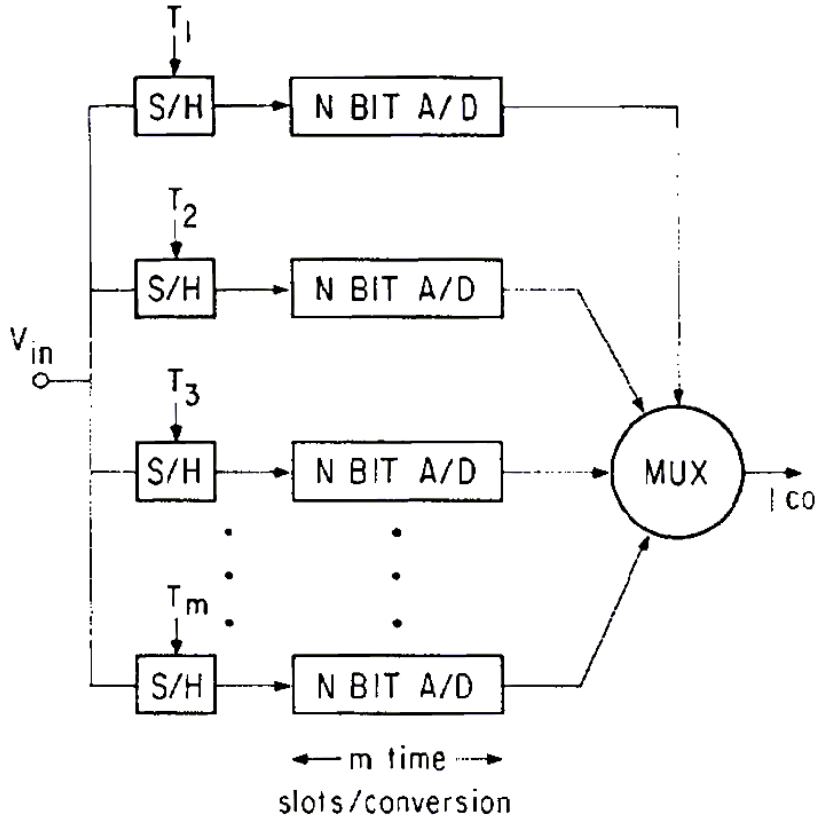
- First known publication on time interleaving (but not an ADC)
- Slice:
  - 200 parallel charge samplers triggered at 40 ns intervals
  - CCD shift register shifts out the analog samples slowly
- Off-chip ADC
- Four slices interleaved for 100 MSa/s total
- Correction for interleaving errors and CCD charge transfer effects
  - Captured waveform recycling
- 6 effective bits up to 30 MHz



"A 100 MS/s Waveform Digitizer with Comprehensive Error Correction", John Corcoran, Tom Hornak, 1980

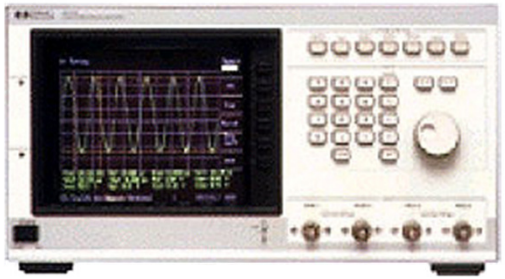
1980: First Interleaved ADC

- Slice: 7-stage SAR pipeline at 0.625 MSa/s
- Four-way interleaved for 2.5 MSa/s
- Implemented in 10 um CMOS
- 6.2 effective bits at 100 kHz in
- Identified and analyzed effects of offset, gain and timing mismatches

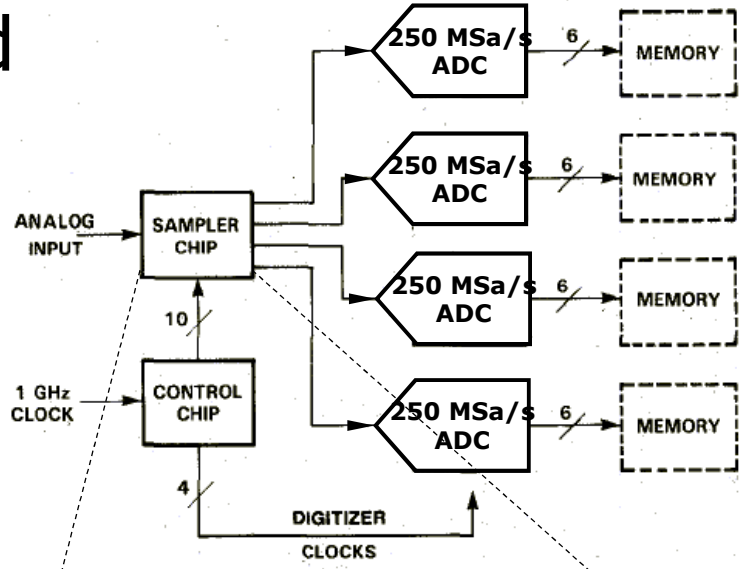


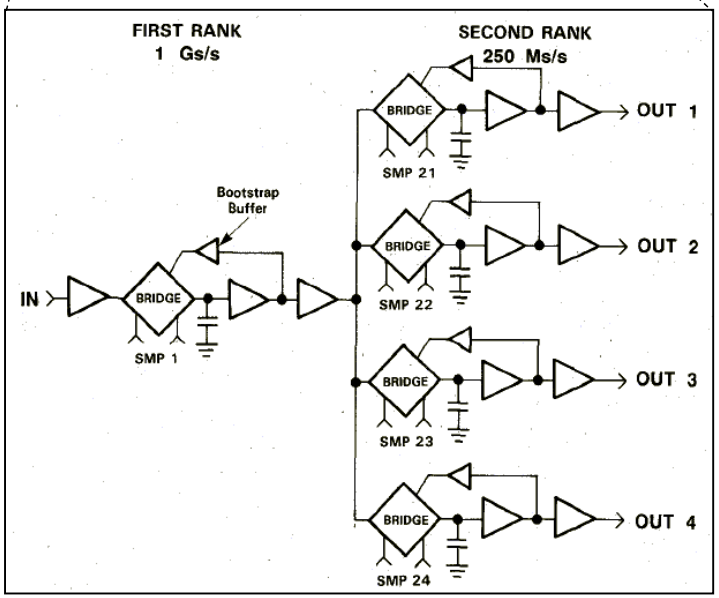
"Time interleaved converter arrays", Black, W., Jr. ; Hodges, D., ISSCC 1980 and JSSC 1980

1987: The First Interleaved ADC Product



- HP 54111D Digital Oscilloscope
- Approach
  - 6-bit bipolar ADC at 250 MSa/s
  - 4-way interleaving
  - 2-rank GaAs T/H chip
  - Custom NMOS memory chip
  - Mix technologies for speed vs complexity
- Mismatch control
  - Offset and gain alignment DACs
  - Single front-end sampler avoided timing calibration





"A 1 GHz 6-bit ADC System", Ken Poulton, John J. Corcoran, Thomas Hornak, IEEE Journal of Solid State Circuits, Dec 1987

Gaining Resolution From Interleaving

Limitations of 6-bit ADC resolution

– 6-bit LSB steps visible on the display

– Better DC resolution desired

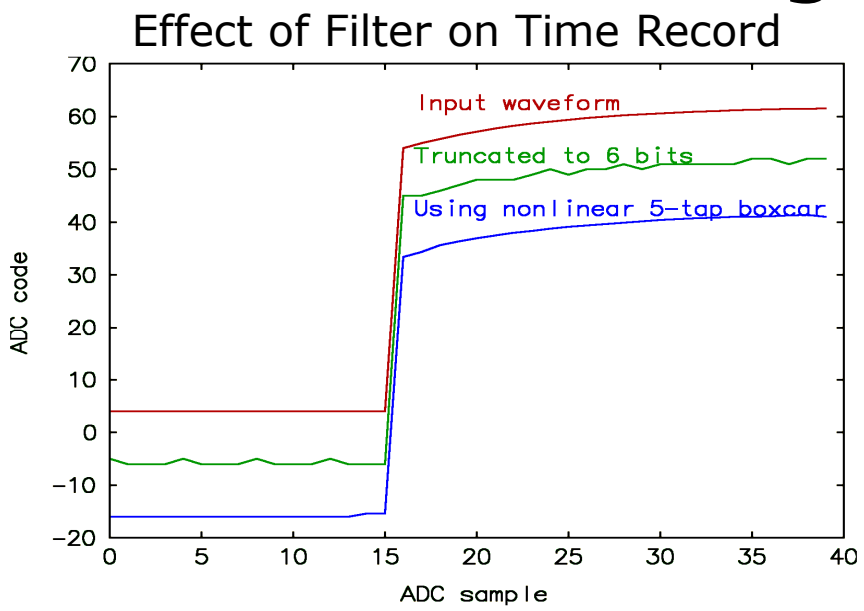
Solution:

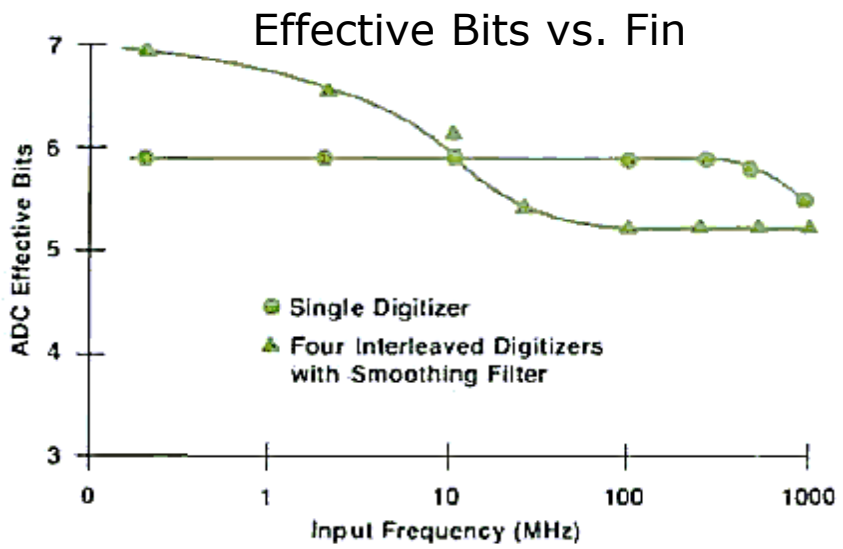
1. Offset the 4 ADCs by ¼ LSB each
2. Apply a nonlinear boxcar filter:
   - Compute linear 5-tap boxcar
   - Limit the change to 0.5 LSB from the original value

Issues:

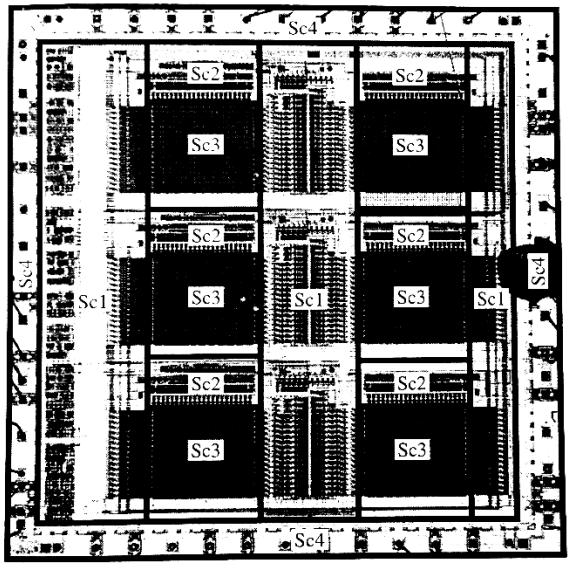
– "preshoot" on steps, quenching of fast near-LSB signals

Not needed in 8-bit scopes



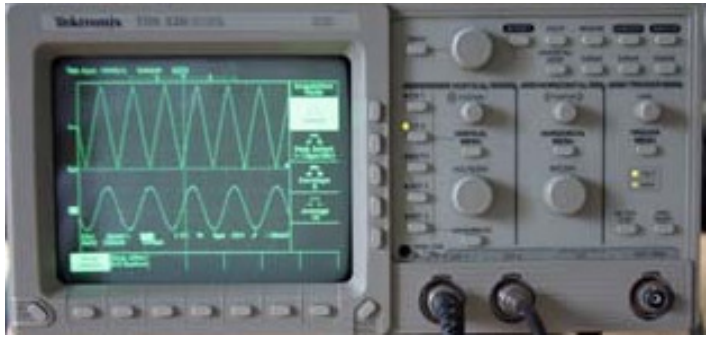


Analog Storage Products



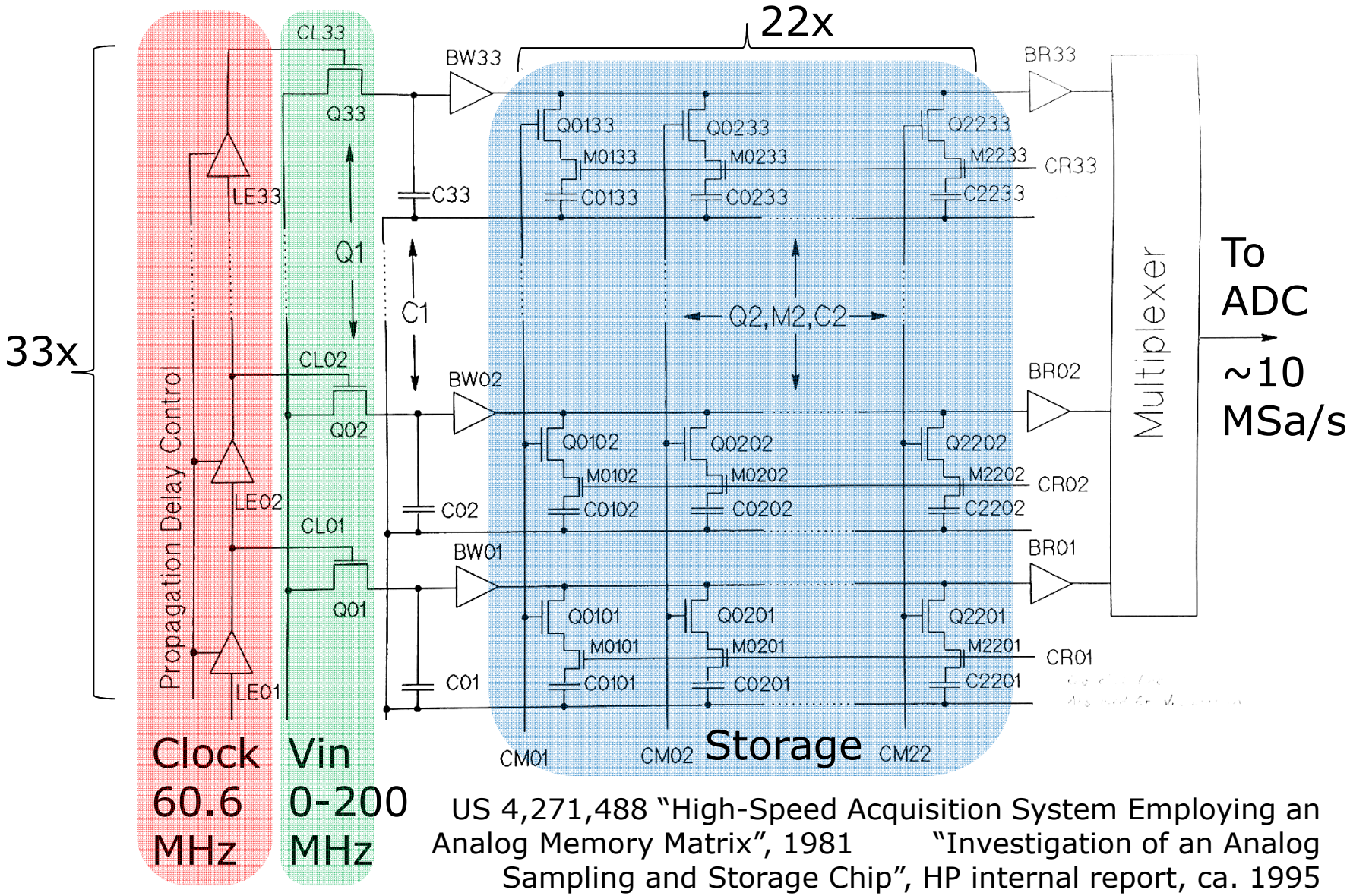
- Analog storage chip
  - 33 interleaved samplers
  - 60.6 MHz clock -> 2 GSa/s
  - 22 storage caps per sampler
  - 2178 samples
- Readout to external ADC ~10 MSa/s

- ~1991: Tektronix TDS 350 Scope
  - 200 MHz BW = high end
  - 1 GSa/s, 2 channels
  - 180 ps pp timing errors
    => ~4 eff bits at 200 MHz



- Today: handhelds apparently still use analog storage
  - 200 MHz BW = low end
  - 1.25 GSa/s
  - 10,000 samples

Analog Storage Chip Schematic



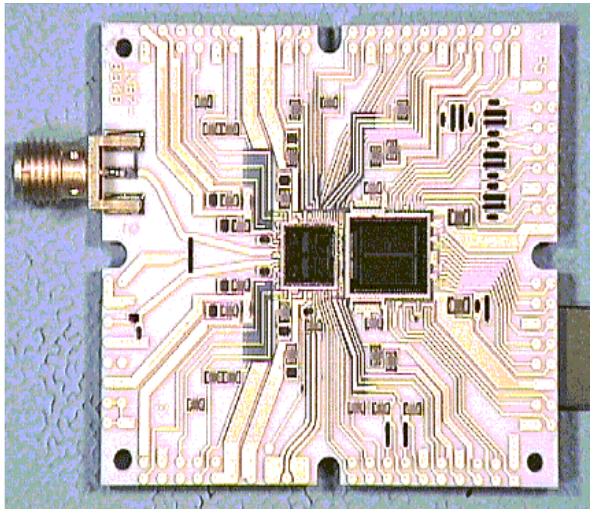
US 4,271,488 "High-Speed Acquisition System Employing an Analog Memory Matrix", 1981 "Investigation of an Analog Sampling and Storage Chip", HP internal report, ca. 1995

Interleaved ADCs in the 90s

- Mostly for Scopes
- Bipolar ADC
  - High Speed
  - Threshold Accuracy
- Low transistor count
  - Yield
  - High power per transistor
- High slice sample rate
  - Time-interleaving of 2-8 unit ADCs
- Front-end T/H topologies:
  - Diode Bridge
  - Switched Emitter Follower
  - Sample + Filter
- High Power
- Custom Packaging

E.g.: 1997 4 GSa/s Module

- 4 GSa/s, 7-bit bipolar ADC
  Folding + Interpolating
- 2-way interleaving on chip -> 4 GSa/s
  4-way interleaving on PCB -> 8 GSa/s
- Custom CMOS Memory
- Thick-film package,13 W, expensive



Timing Calibration Methods

- S. Takeuchi, et al (Sony/Tektronix) used sawtooth waveforms
  - Hard to make accurate at high frequencies
  - "Analog-to-digital conversion method and apparatus", US 4345241, Aug 1982
- H. Katusmata (Sony/Tek) used pulse waveforms at a beat frequency where each slice sampled the same voltage on the waveform
  - Only uses the zero crossing information, needs precise control of the cal frequency.
  - H. Katsumata, et al, "Method and apparatus for calibrating an analog-to-digital conversion apparatus", US 4736189, Apr 1988
- John Corcoran (HP) used the two-rank T/H architecture to avoid timing calibration
  - Requires a full-rate sampler that adds power, noise, distortion
- Y.C. Jenq (Tektronix) used a DFT-based method
  - Uses DFT of the waveforms. Needs precise control of the cal frequency.
  - "Interleaved digitizer array with calibrated sample timing", US4763105, Jul 1987
- John Corcoran (HP) devised a way of measuring timing and amplitude errors based on per-slice best-fit analysis.
  - Allows a non-frequency-locked cal source for low-cost instrument self-cal.
  - "Timing and amplitude error estimation for time-interleaved analog-to-digital converters", US 5294926, 15 Mar 1994

Some Scope ADCs in the 90s

- HP in 1991
  - 500 MSa/s per slice, 1 GSa/s per chip, 13-GHz silicon BJT, folding ADC
  - 4, 8-way interleaved to up 4 GSa/s

    Rush & Byrne, "A 4GHz 8b Data Acquisition System", ISSCC 1991
- HP in 1994
  - 4 GSa/s, 6 bits, 50-GHz GaAs HBT, folding ADC
  - Did not go into a product

  Poulton, et al, "A 6-bit, 4 GSa/s ADC Fabricated in a GaAs HBT Process",1994 GaAs IC Symposium
- HP in 1997
  - 2 GSa/s per slice, 4 GSa/s per chip, 7 bits, 25-GHz silicon BJT, folding and interpolating
  - 2, 4-way interleaved to 8 GSa/s

  Poulton, et al,"An 8-GSa/s 8-bit ADC System", VLSI Symposium, 1997
- Other scope manufacturers
  - developed bipolar ADCs, but did not publish
  - followed the fast-slice, low-interleaving paradigm

Calibration and Correction Choices

- Corrections = analog and digital circuits that improve the accuracy
  - E.g., Voltage adjust DACs, delay DACs, DSP
- Calibrations = the processes that set the correction parameters

- To Cal or Not To Cal
  - Accurate by Design (no calibration and correction)

    -- Full matching and linearity requirements must met by design
  - Calibration and Correction

    + Can relax analog performance requirements

    + Analog circuits can be limited only by SNR, not matching
      - Smaller, lower power circuits

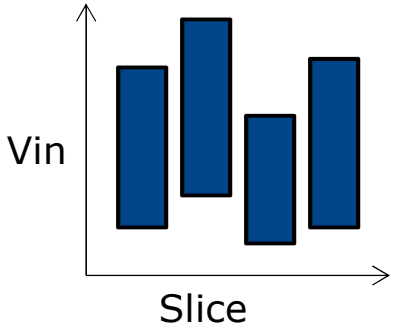
    -- Added power for correction circuits

    -- Added complexity for corrections and for calibrations

Analog vs. Digital Corrections

As fabricated:

Usable analog range of each slice is different

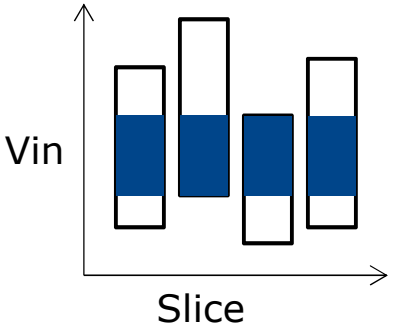


Digital correction:

Use only the voltage range that overlaps in all slices.

+ Calibration is digital and simple

-- SNR and resolution degraded

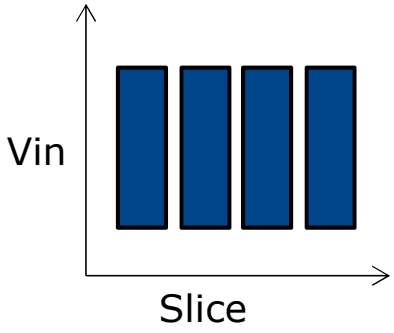


Analog correction:

DACs adjust the offset and gain of all slices to match

+ Preserves slice ADC resolution and SNR

-- More analog circuits to design



Correction Circuits

- Offset and gain corrections are simple in digital: just an adder and a multiplier per slice.

- Timing corrections in digital circuits require a delay filter
  - Bandwidth limited (e.g., 80% of Nyquist)
  - Significant complexity and power
- Timing corrections in analog require variable delays
  - Power can be high, proportional to delay/jitter

- Either analog or digital *or both* can be used
- More digital has been used in recent years

Calibration Choices

- On-chip vs off-chip calibration (parameter computation)
  - Off Chip:
    + lower chip cost
    + lower design risk
  - On Chip
    + Simpler for the ADC user

- Foreground calibration vs. Background calibration
  - Foreground (offline)
    + Independent of the input signal
    -- ADC user needs to provide cal signals
    -- Dead time during calibration
  - Background (online)
    + Can be simpler for ADC user
    -- More complex chip
    -- Often places requirements on the input signal characteristics

"A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration", Shafiq Jamal, et al, JSSC, Dec 2002, pp1618-1627

IC Process Trends in the 90's

- Consolidation of fabs
  - In 1990, lots of captive IC fabs (e.g., 10 fabs in HP)
  - Late 1990's: $1B fab cost squeezed out many players
  - Rise of commercial foundries with leading-edge CMOS
- Bipolar and BiCMOS
  - Increasingly a niche technology, focused on performance
  - Investment driven by specific market trends
    - ~1990: CPUs, ~2000: RF, ~2010: 25+ Gb/s comms & uW
    - Investment fades as CMOS gets fast enough for a given application
    - => Less predictable progress in bipolar
- CMOS
  - Following Moore's Law
  - Lower wafer costs
  - Higher integration can reduce system costs
  - More predictable progress in performance

Could We Use CMOS for Scope ADCs?

- "Don't be stupid"
  - CMOS ADCs (ca 1995) were 25x slower than bipolar
  - CMOS transistors are 10 times less accurate than bipolars
- "But..."
  - CMOS chips are cheap and transistors are virtually free
  - Could integrate with DSP and memory
  - Might be lower power

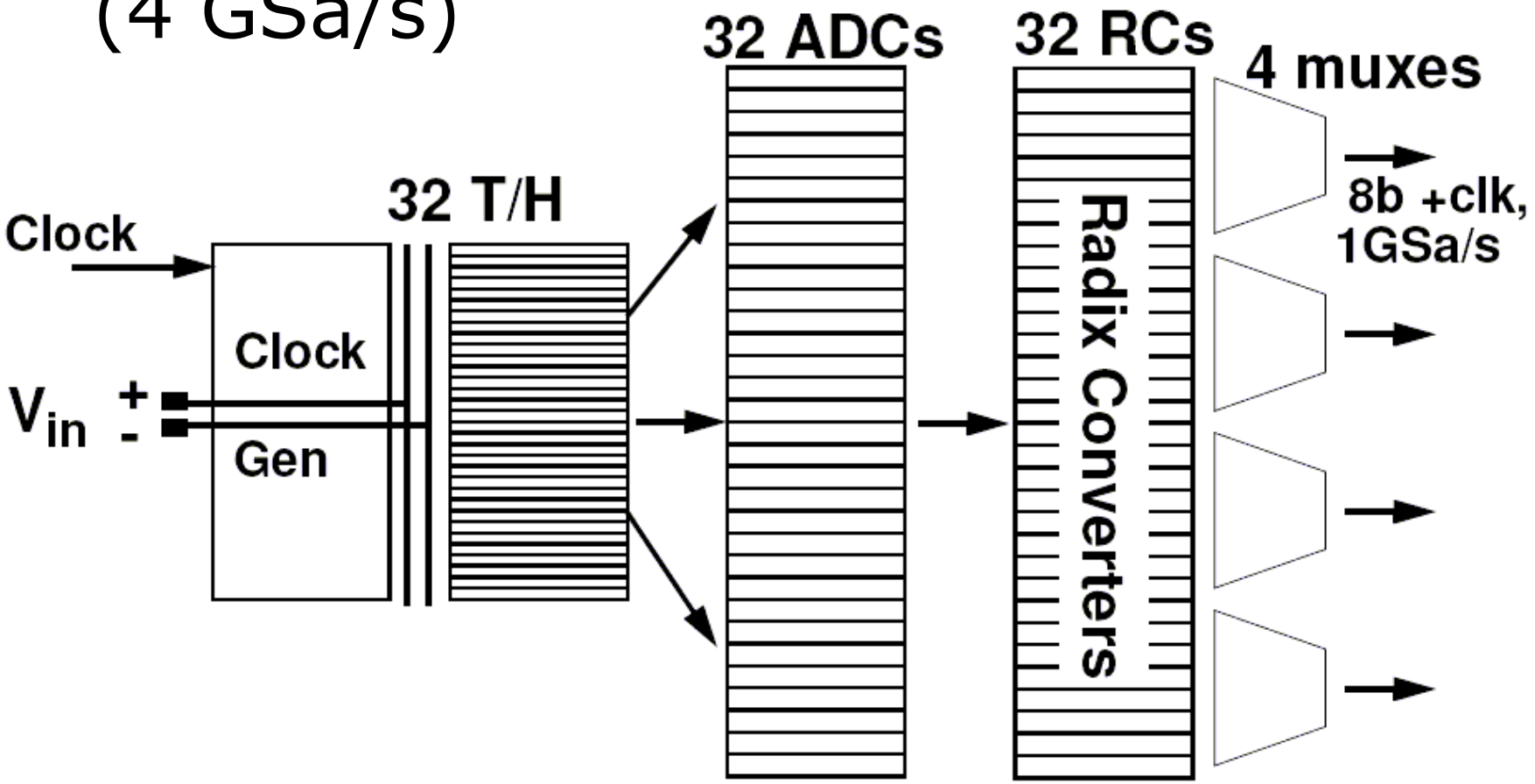
"If we don't do [ADCs] in CMOS, someone else will."
-- Dave Robertson, ADI, ISSCC ca 1995

Architecture: Massive Interleaving of Low-Power ADCs

- Focus on the strengths of CMOS: low power and high integration
- Start with a power-efficient CMOS ADC slice
- Time-interleave like crazy to get the required sample rate
- Fix up analog accuracy through calibration

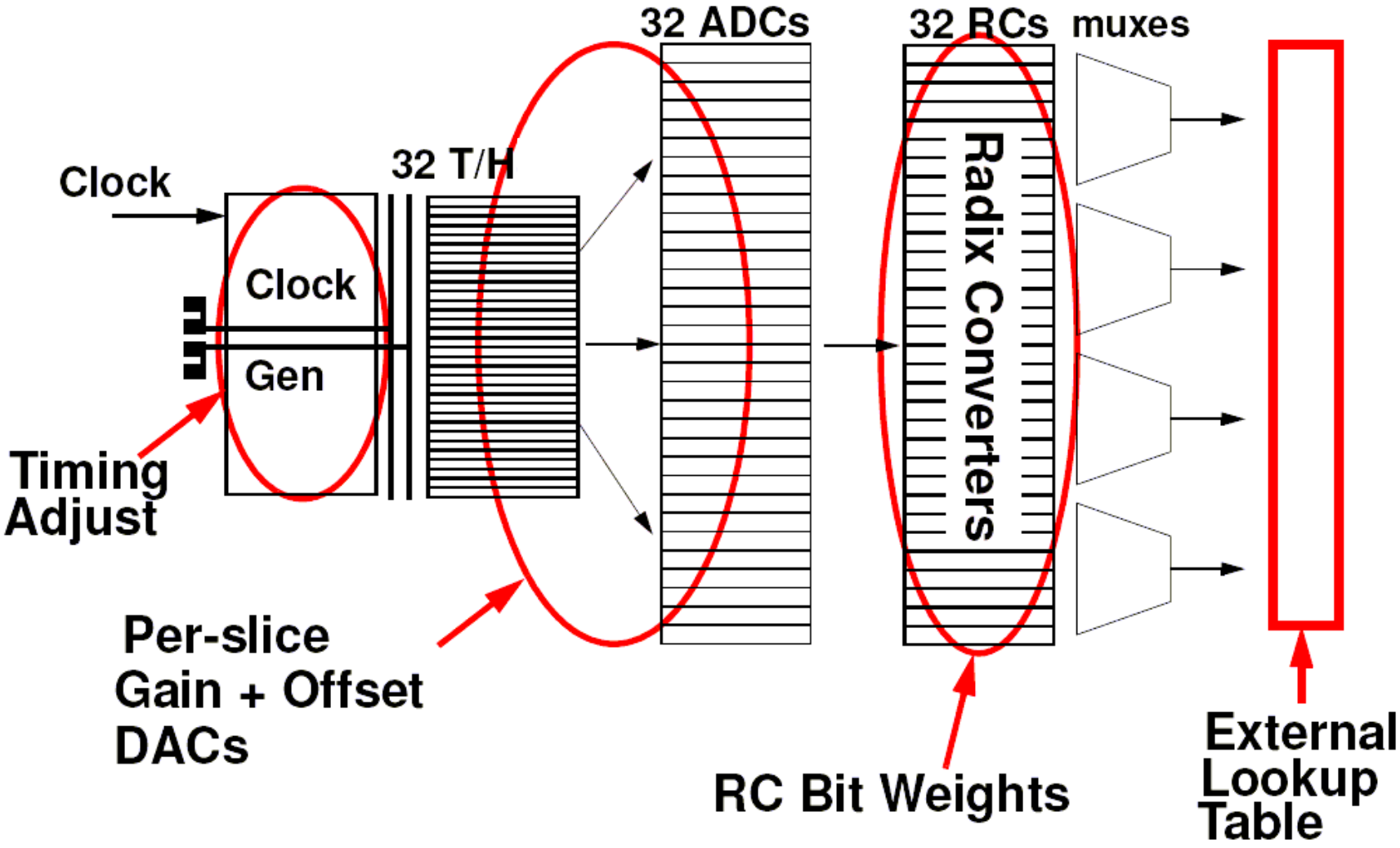
- Challenges:
  - Track/Hold : Bandwidth, Signal distribution
  - Clock generation
  - ADC: Trading Sample Rate, Power, area, # of slices
  - Many Places for Mismatch

2002: CMOS ADC Chip Architecture (4 GSa/s)



- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s

What Is Calibrated?



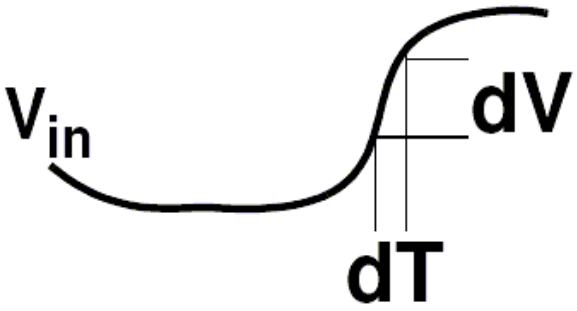
- Foreground (offline) Calibration with DC and Pulse sources

Advantages of a Calibration Approach

- Device mismatch tolerance increased
  - In this case, from ~0.25% to ~10% mismatch
  - Can design for SNR rather than mismatch
  - Smaller transistors
  - Lower power
- Second-order effects can be covered by the same calibrations
  - Smaller device mismatch effects (e.g., layout-related delta W)
  - Delay and gain mismatches due to layout asymmetries
- Adjust DACs need not be tightly matched, merely have enough resolution

Timing Errors

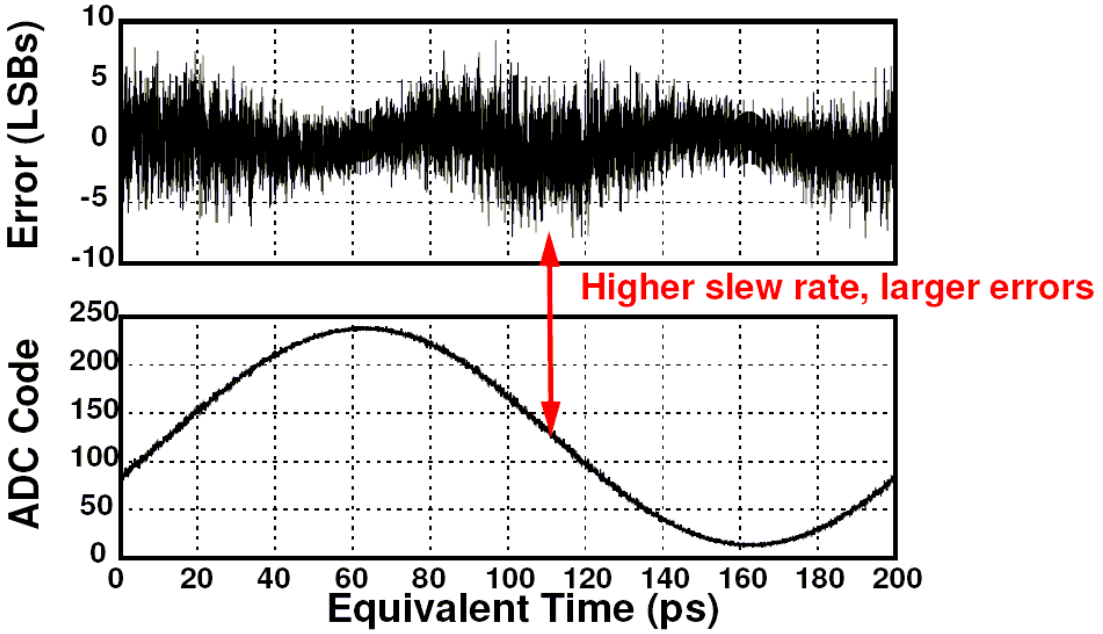
- Fast input signal converts a sample timing error (dT) to an apparent voltage error (dV).



Rule of Thumb:

1 ps rms @ 1 GHz Fin

--> 7 effective bits

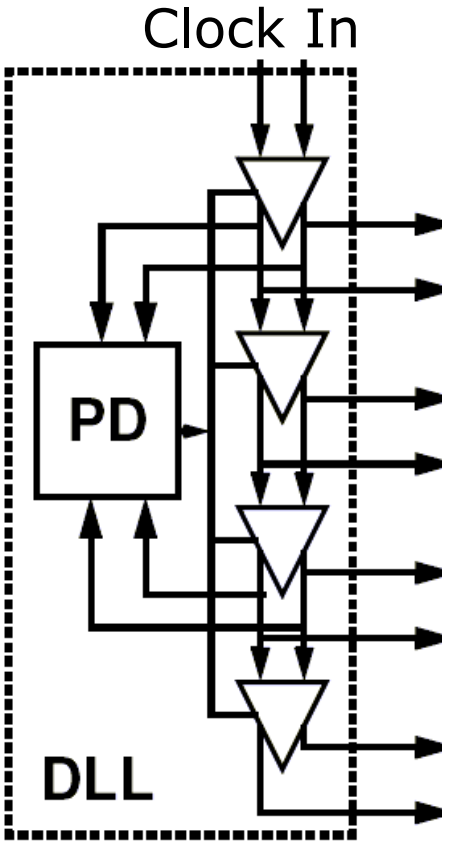


Clocks for Front-End Samplers

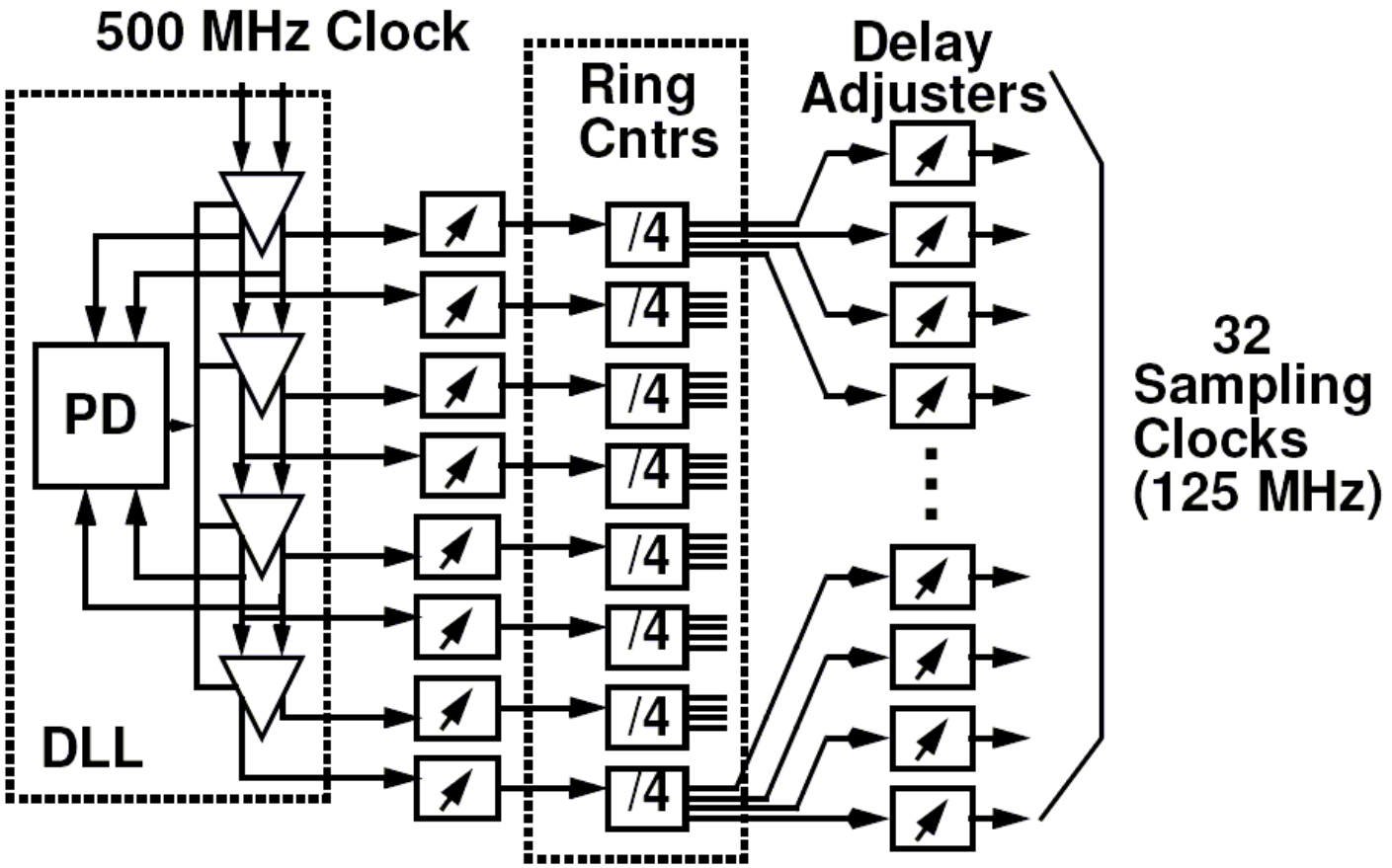
- Single Front-end Sampler
  - **One** low-jitter clock (30-1000 fs rms jitter, dep. on application)
  - N reduced-accuracy clocks (1-10 ps rms jitter and alignment)
    - Second rank requires fairly accurate clocks due to analog settling effects
- Interleaved front-end samplers
  - **N** Full-accuracy clocks
    - 30-1000 fs rms jitter ***and alignment***

Using Lower Input Clock Frequencies

- Full-rate clock
  - Used by earlier bipolar designs
  - Just divide the input clock down to get the slice clocks
  - Low jitter, modest calibration
  - High-frequency clock sources are expensive
- Low-rate clock
  - Fclock << Fs (e.g., 500 MHz << 4 GSa/s)
    - Saves power
    - Full rate just infeasible for some CMOS ADCs
  - N parallel samplers requires N full-accuracy clocks
- DLL for N clocks, constant jitter spec
  - N/2 stages
  - Stage power scales as N to maintain jitter
  - => DLL power scales as N2



Hybrid Clock Generator

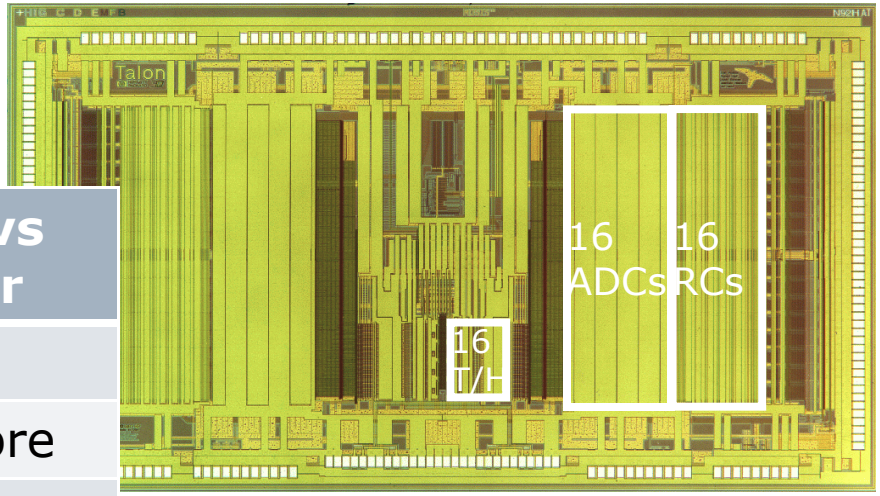


- 4 GSa/s, ~ 1 ps thermal jitter in 0.35 um CMOS
- Timing errors: before cal 10 ps rms, after cal 0.8 ps rms

US 6,956,423 "Interleaved clock signal generator having serial delay and ring counter architecture", Oct 2005, Robert Neff

4-GSa/s 8-bit ADC Results

	CMOS ADC	CMOS vs bipolar
Sample Rate	4 GSa/s	same
Resolution	8 bits	1 bit more
SNDR	7.0 effbits	0.5 bit more
BW	1 GHz	50%
Interleave	32-way	16x more
Transistors	300K	100x
Area	28 mm^2	~75%
Power	4.6 W	1/3
Cost		1/5

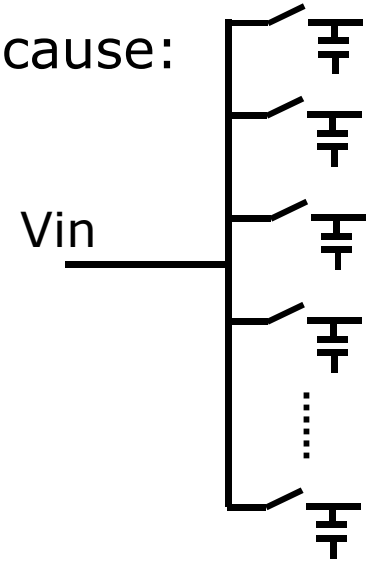


0.35-um CMOS
7.1 mm x 4.0 mm
300,000 FETs
4.6 W

"A 4-GSample/s 8b ADC in 0.35-um CMOS", Ken Poulton, Robert Neff, Art Muto, Wei Liu, Andy Burstein, Mehrdad Heshami, ISSCC, pp 166-167, Feb 2002

Issue: Coping With Wide Inputs

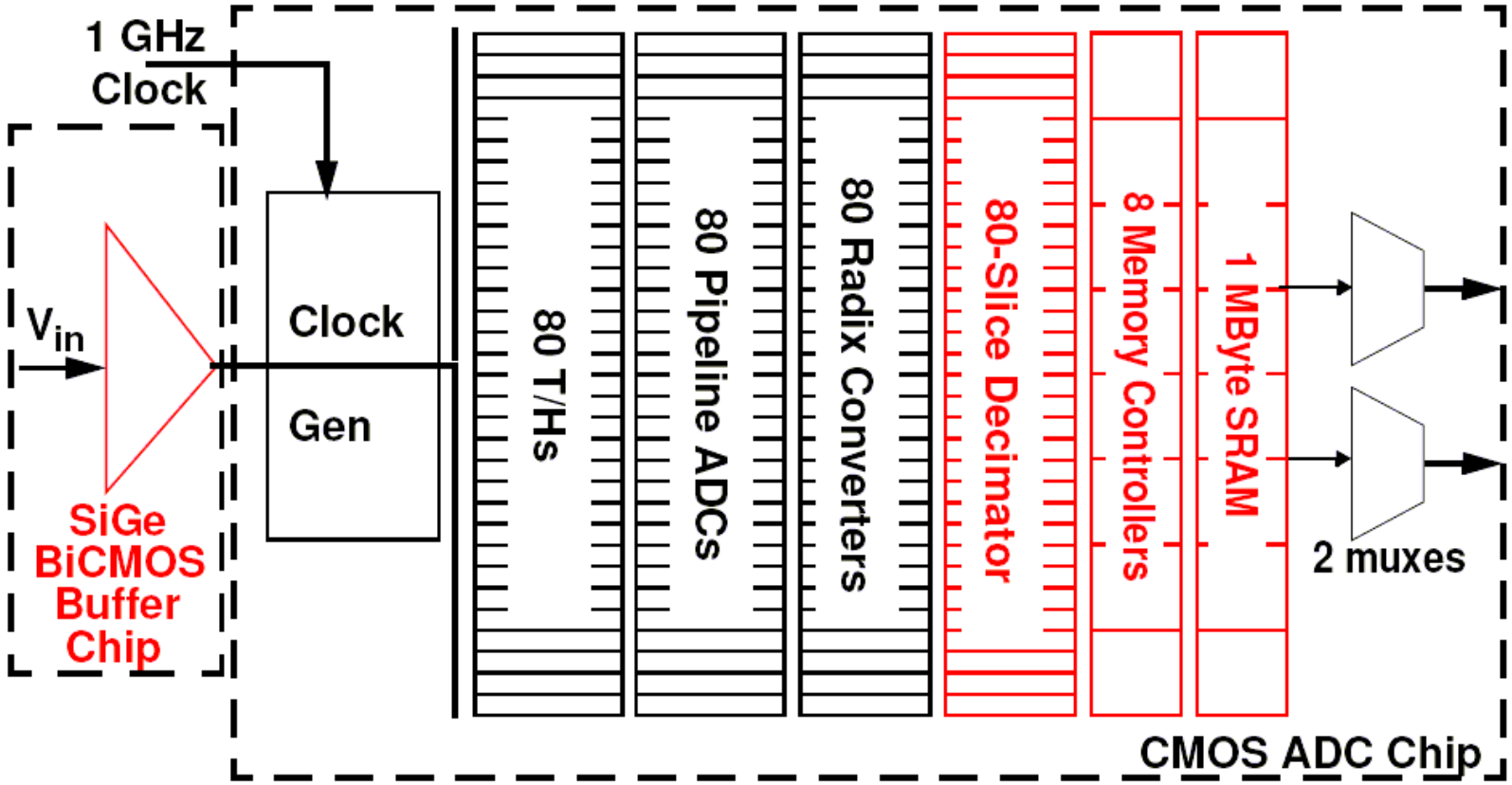
- Many parallel samplers connected to Vin cause:
  - High capacitance, e.g., 2 pF
  - Physical distribution challenges
    - Binary tree has matched lengths, but much more C
- Approaches:
  - Lower the source impedance
    - e.g., 25 ohms Rin
    - Add a buffer amplifier
  - Reduce the sampler count connected to Vin
    - Each sampler feeds multiple ADC slices
    - Each sampler feeds multiple second-rank samplers



Issue: The Digital Firehose

- Current gigasample ADCs spew out 4 to 500 Gb/s
  - I/O power can be as much as ADC power
- Separate Receiver Chip
  - FPGAs with 50+ SerDes can cost $1000's apiece
  - Custom data capture chips cost millions for design
    - Much lower power and per-chip cost
- On-chip storage
  - Can reduce system cost and power
  - Limited memory size
    - Reduces the range of products possible
  - Slower readout leads to ~90+% deadtime
- On-chip DSP
  - Can reduce the data rate by 2-10x for applications such as datacomm

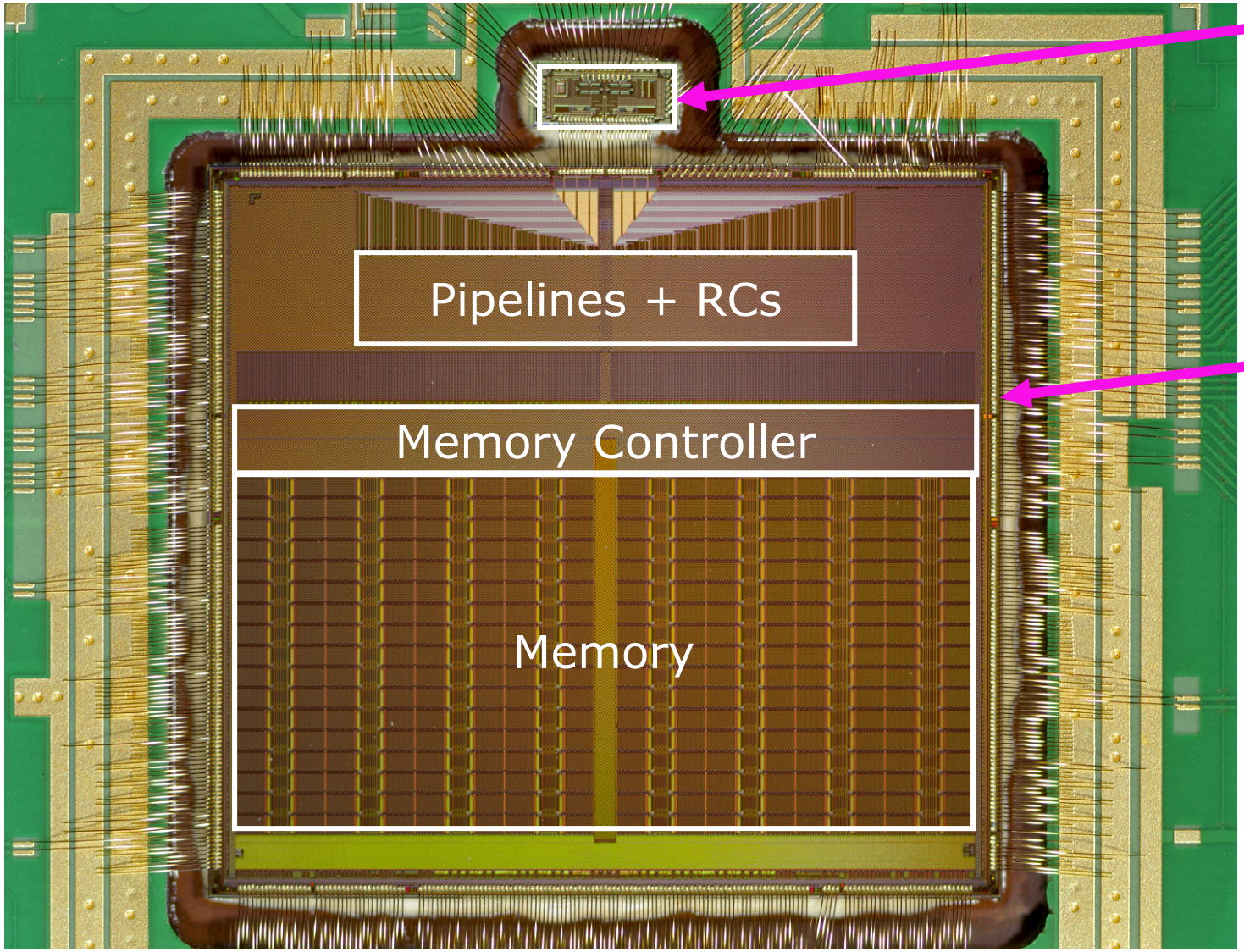
2003: 20-GSa/s 8-bit ADC, 0.18 um CMOS



- 2x faster process, 5x higher sample rate, 6x higher BW
- 80 ADC slices, larger Cin --> SiGe input buffer chip
- 160 Gb/s data rate --> 1 MB on-chip sample memory

"A 20 GS/s 8 b ADC with a 1 MB memory in 0.18-um CMOS", Poulton, Neff, Setterberg, Wuppermann, Kopley, Jewett, Pernillo, Tan, Montijo, ISSCC, pp 318-319, Feb 2003

20 GSa/s ADC Module

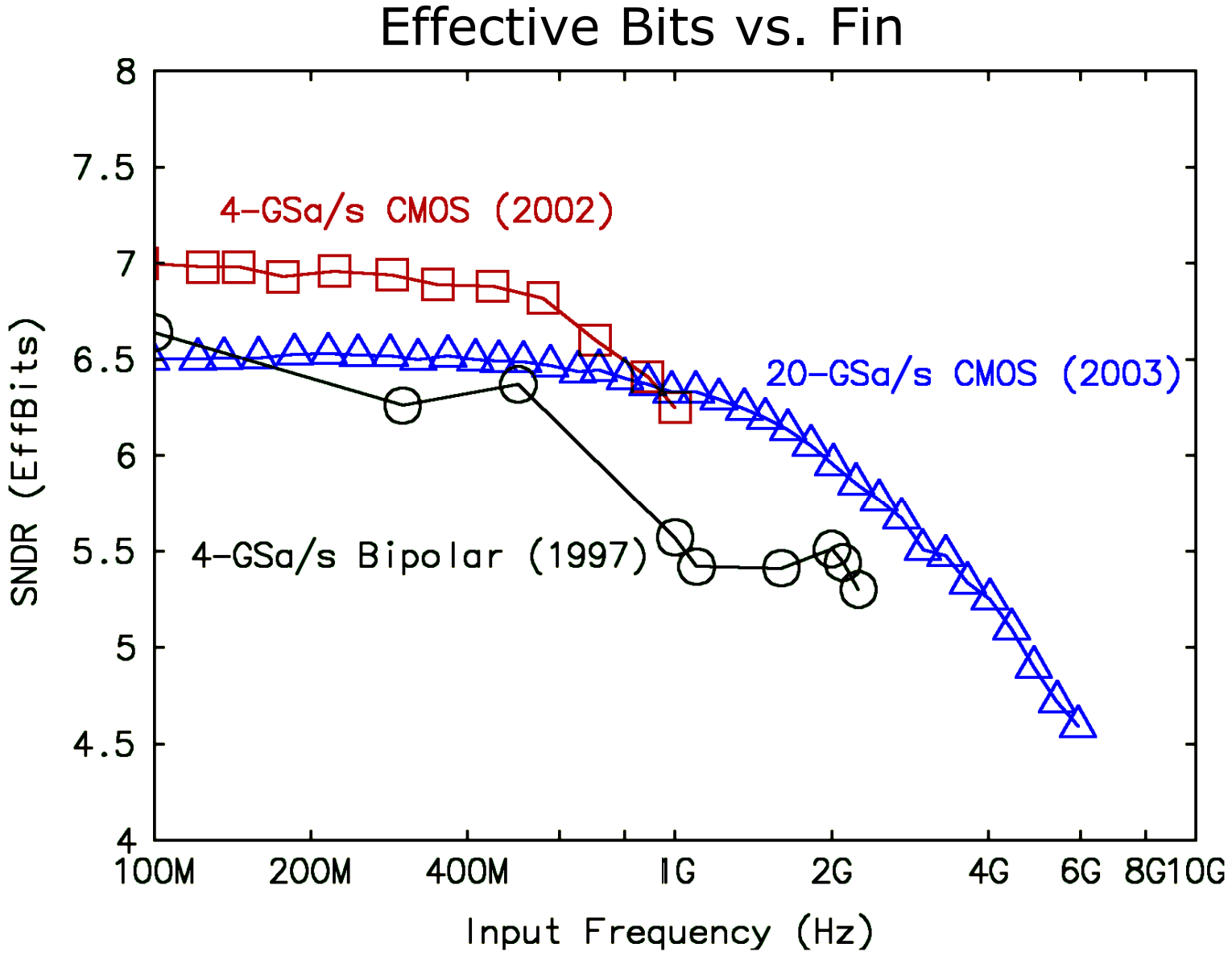


Buffer:
40 GHz SiGe
1 x 2 mm
1000 transistors
1 W

ADC:
0.18-um CMOS
14 x 14 mm
50M transistors
9 W

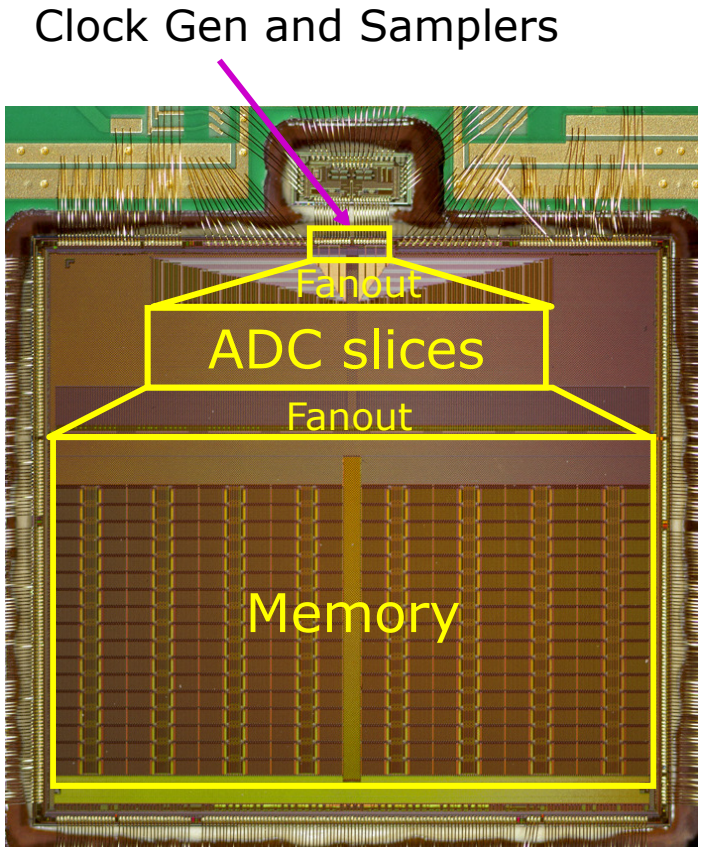
Package:
438-ball BGA
35 x 35 mm

Performance of Bipolar and CMOS ADCs



Issue: Clock and Signal Distribution

- Multiple samplers requires distributing clocks
- Tradeoff between dense samplers and larger size of the ADC slices
- Both clock and analog signal distribution can take a lot of area and power
- Example: 80-slice ADC:
  - samplers: 1.9 mm wide
  - ADCs: 9 mm
  - Memory 13 mm



Other Issues for Massive Interleaving

- Frequency-dependent mismatch
  - Small BW mismatches can be mostly corrected as timing mismatches
  - Larger BW or rolloff shape mismatches won't work this way
    - Electromagnetic modeling of Vin distribution network
    - Digital time-varying filter can provide correction **
- Kickback into analog input
  - When a T/H reconnects to the input, kickback (from previous sample) is injected into the input network
    - Can cause an "echo" from ~N samples earlier
    - Can create a high-slew disturbance while another T/H is sampling
- Crosstalk among slices
  - Power supplies and shared bias lines
  - Clock networks
  - Analog sample fanouts

** "A Polynomial-Based Time-Varying Filter Structure for the Compensation of Frequency-Response Mismatch Errors in Time-Interleaved ADCs", Johansson, IEEE Sig Processing, 2009

Time Interleaving for High Dynamic Range

- Application area: RF receivers
- Key Specs for instruments

	Scopes	*RF Instruments*
SFDR	40-50 dB	60-80 dB
SNR	~7 bits	~10 bits
BER**	1/year	1/year

** BER = Bit Error Rate = Metastable Error Rate

- Instruments require very low rates, e.g., 10^{-17}
  - Due to peak detect mode
- Communications channels can allow rates as high as 10^{-8}
  - Use of DSP and error correction

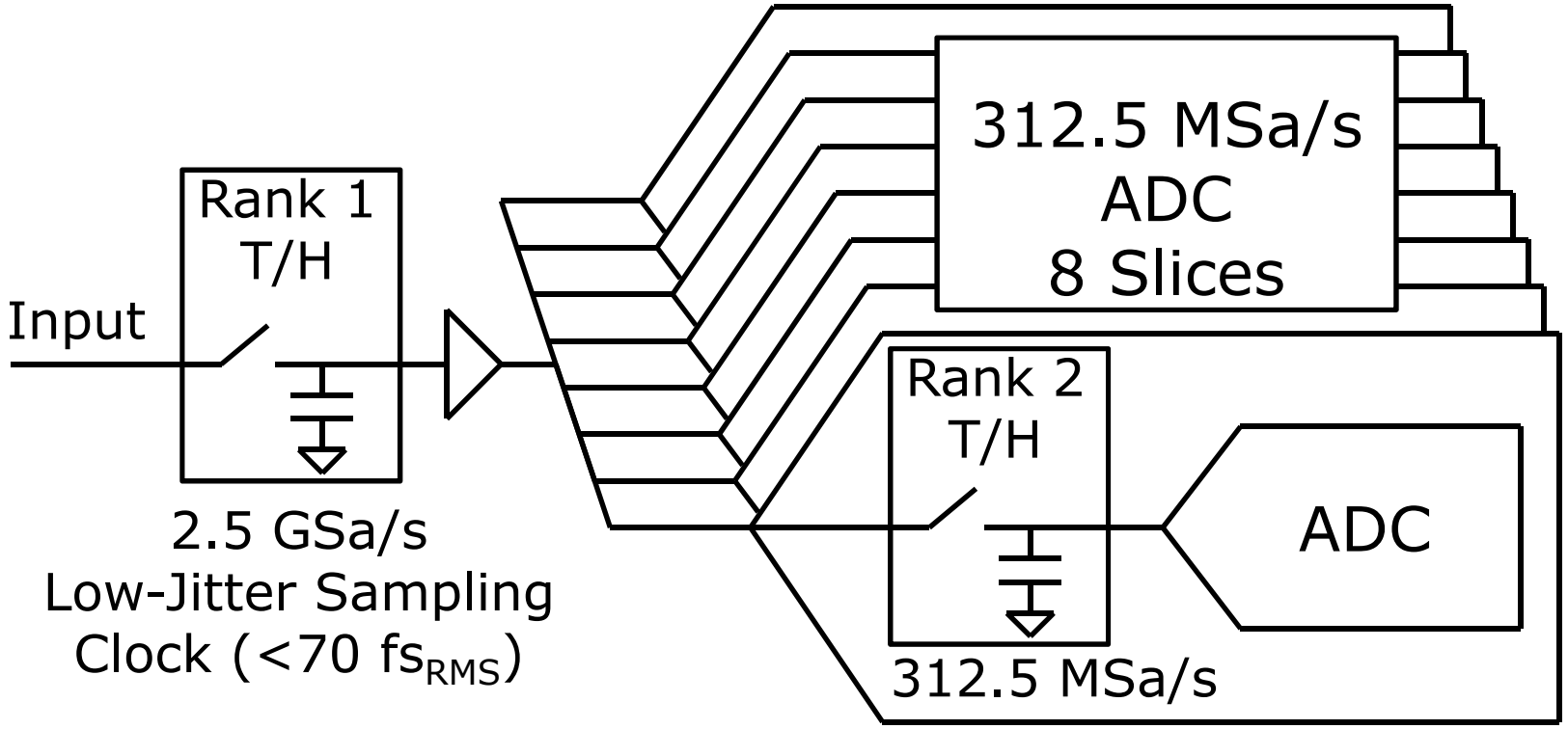
A 14-bit 2.5-GSa/s 8-Way-Interleaved ADC

Goals and resulting design decisions

- 10^{-17} Metastable error rate
  - Interleaved
  - Low slice sample rate (312.5 MSa/s), 8 slices
- 80 dB SFDR
  - Single full-rate first sampler to suppress timing mismatch
  - Background calibration for gain and offset mismatch
  - Digital Dynamic Linearity Corrector (DLC)
- 60 dB SNR
  - Background calibration for pipeline inter-stage gain parameters
- No assumptions about input signal
  - Background cal injects its own dither signals

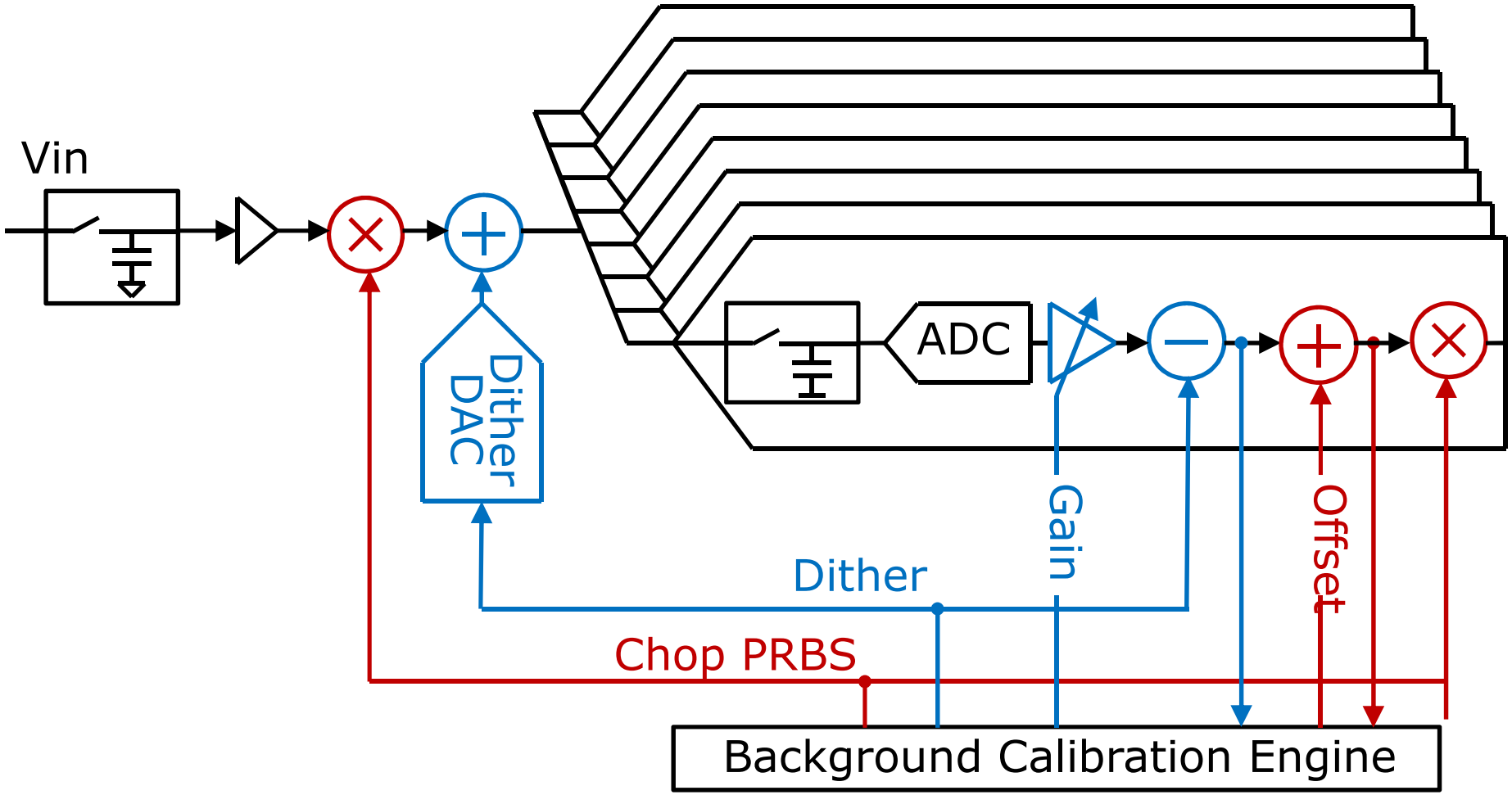
"A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction", Setterberg, et al, ISSCC 2013

Minimize Sampling Time Errors with a 2-rank Track and Hold



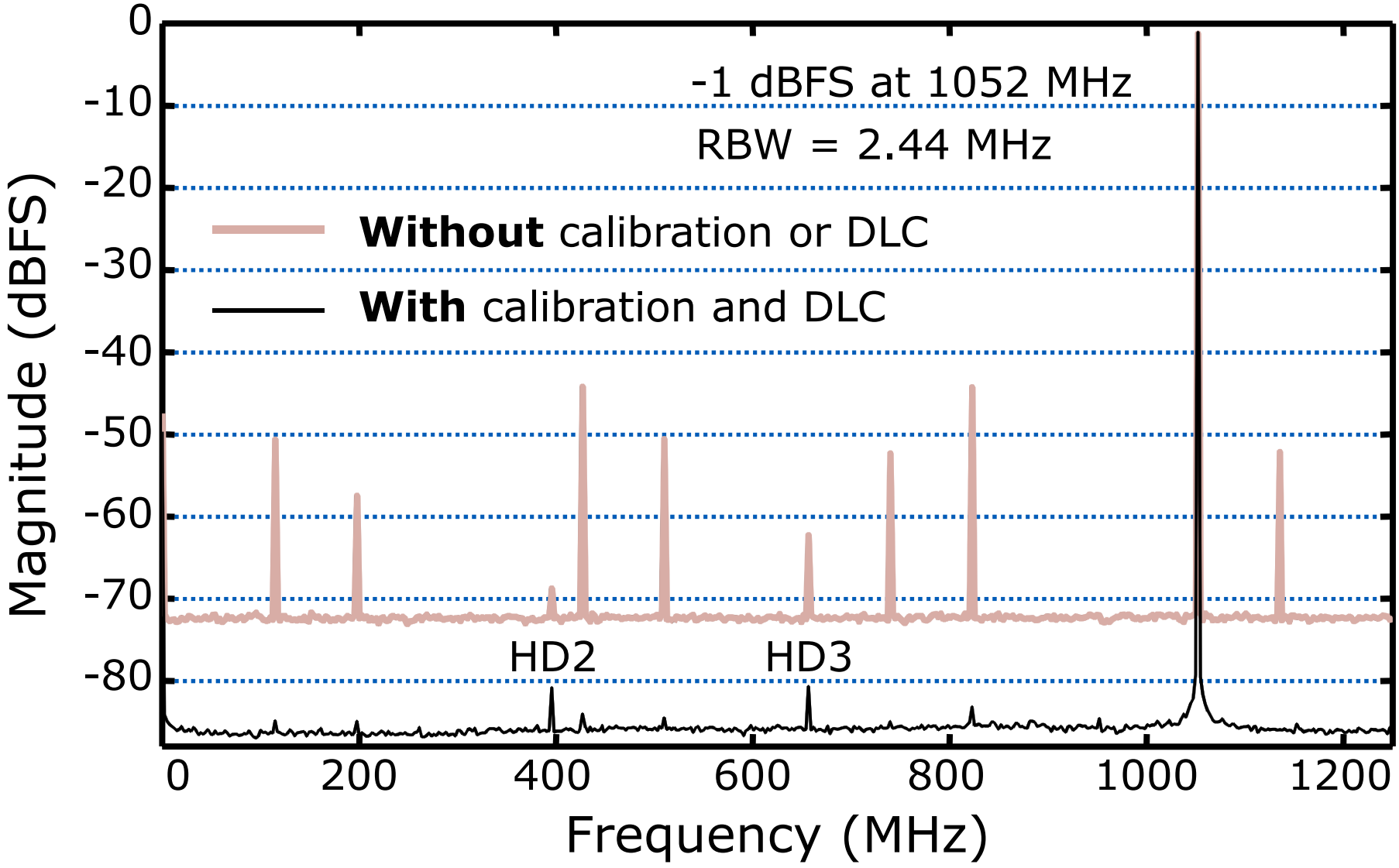
- Sample timing defined by first T/H

Slice-to-Slice Gain & Offset Alignment

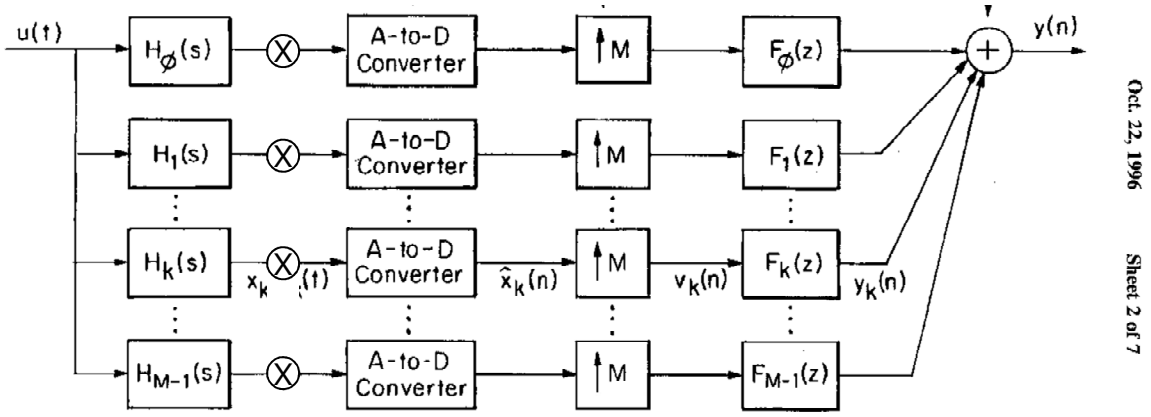


- Injected dither provides an absolute gain reference
- Chopping allows offset calibration
- Both are independent of the input signal

Power Spectrum



Frequency Interleaving (Early 90's)



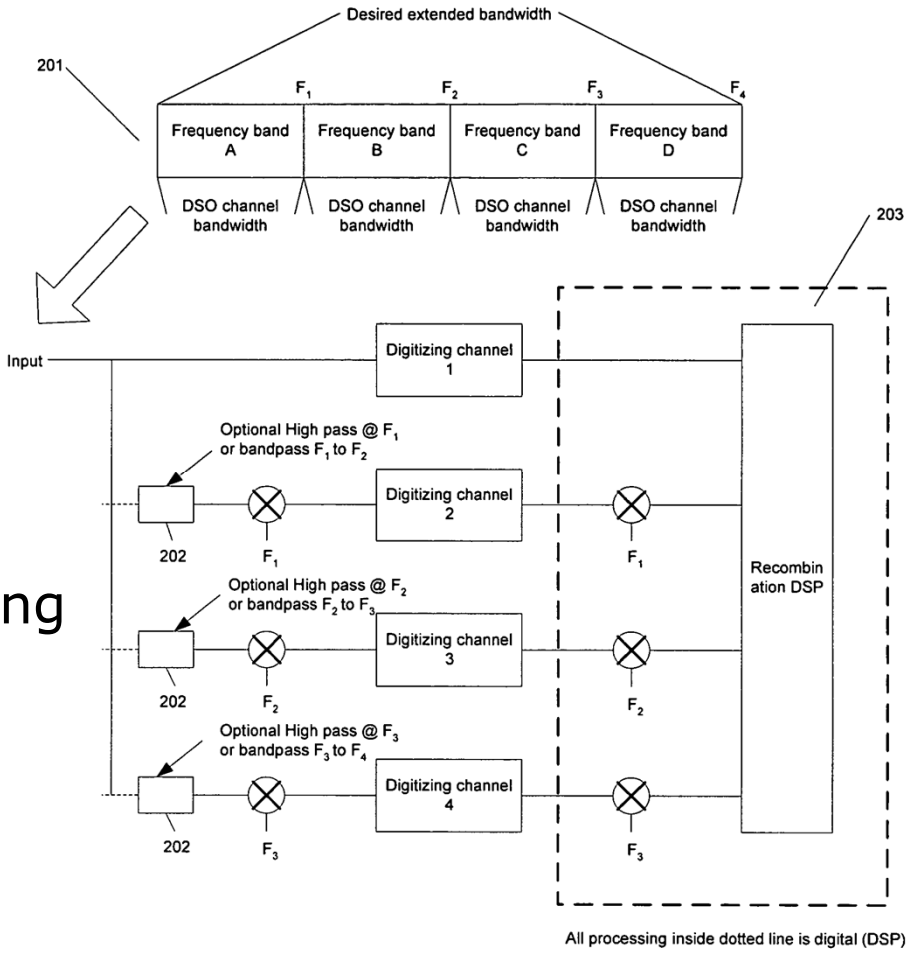
- Basic Idea
  - Use filters to separate input into one frequency band per channel
  - Mix each channel down to baseband
  - Perform A/D Conversion and combine channels
- Pros and cons vs. time interleaving
  - \+ Reduced jitter sensitivity for ADC clocks
  - \+ Some ADC noise and distortion can be filtered out after the ADC
  - -- Filters and mixers don't integrate well
  - -- Tricky to align band edges, especially in phase

"High speed A/D Conversion using QMF banks", A Petraglia, S.K. Mitra, ISSCC 1990

"System for converting a signal between continuous-time and discrete-time", US 5568142, Velazquez, Nguyen, Broadstone, Oct 1994

First Frequency Interleaving Product

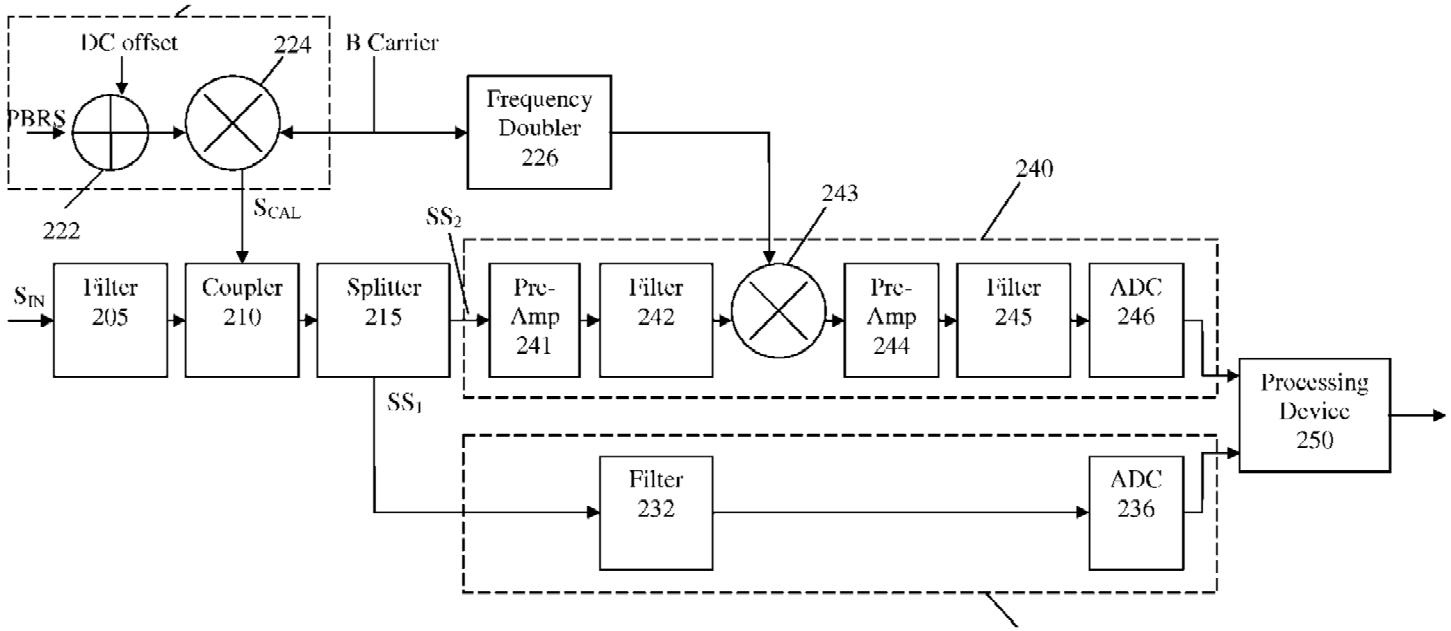
LeCroy SDA 11000 2005
- Two 6-GHz slices
- 2-way frequency interleaving
- 11 GHz, 40 GSa/s



"High bandwidth real-time oscilloscope", US 7058548, Peter J. Pupalaikis, David C. Graef, June 2006

Cal Methods for Frequency Interleaving

- LeCroy describes using phase-locked tone(s) in crossover region
  - foreground cal
- Keysight describes using a PRBS comb in the crossover region
  - allows background cal

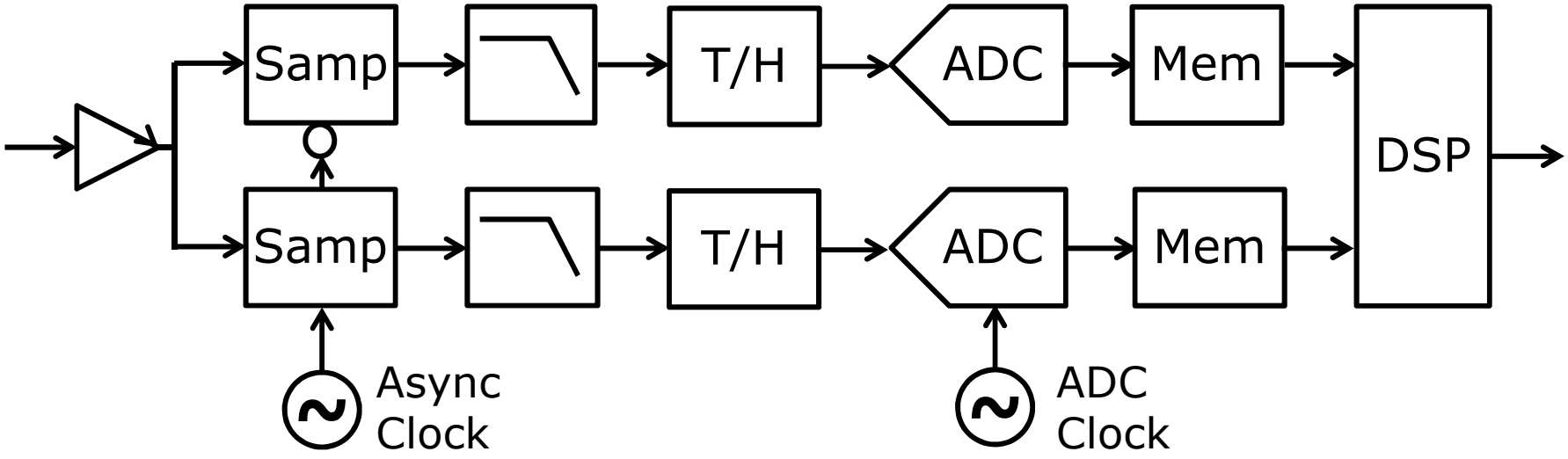


"Method of crossover region phase correction when summing signals in multiple frequency bands", US 7711510, Pupalaikis, et al, May 2010
"Calibrating reconstructed signal using multi-tone calibration signal", US 8849602, Ken Nishimura, Ken Rush, Oct 2014

High End Products

- Keysight 63 GHz BW 2-way freq int Shipped in 2012
- LeCroy 100 GHz BW 3-way freq int 2015?
- Tek 70 GHz BW 2-way ATI 2015?

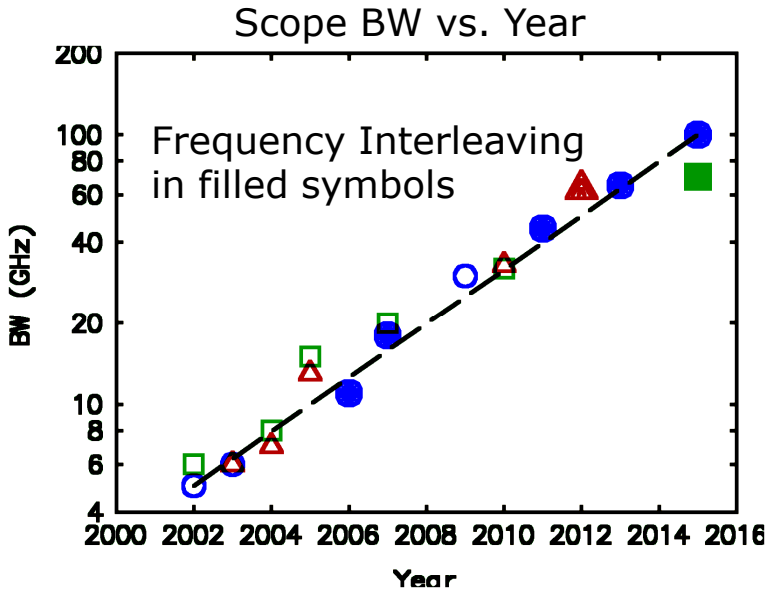
- Tek Asynchronous Time Interleaving (ATI):
  - Upper-half frequencies are aliased into two baseband channels with two phases of an asynchronous clock.

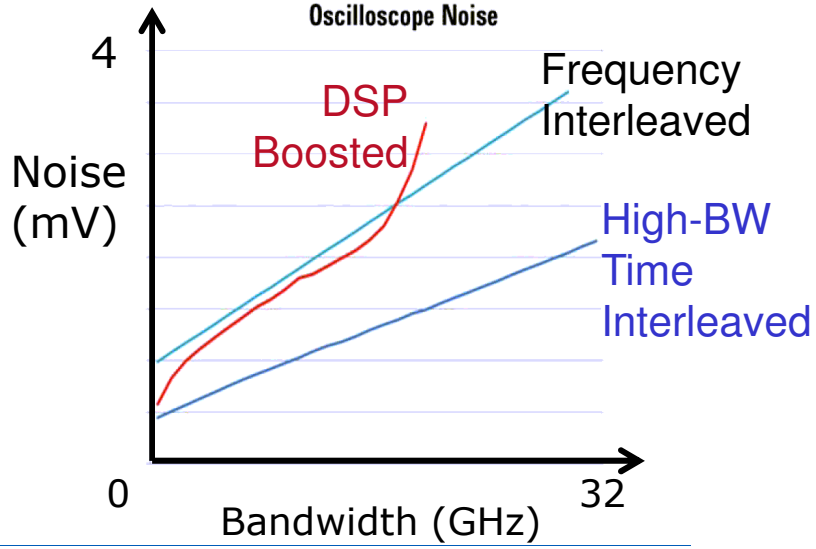


"Techniques for Extending Real-Time Oscilloscope Bandwidth", tek.com, 2013

Frequency Interleaving in Scopes

- Scope BW bandwidth has been doubling every 2.8 years
  - Frequency interleaving hasn't changed that
- Cost of high-end scopes near $10K/GHz/2-channels for 10 years
  - Due to small volumes, increasing scope complexity and increasing chip NRE
- In 30 GHz oscilloscopes, the time-interleaved scope had substantially lower noise than the frequency-interleaved scope.
  - Comparative data not available for the 60+ GHz scopes yet





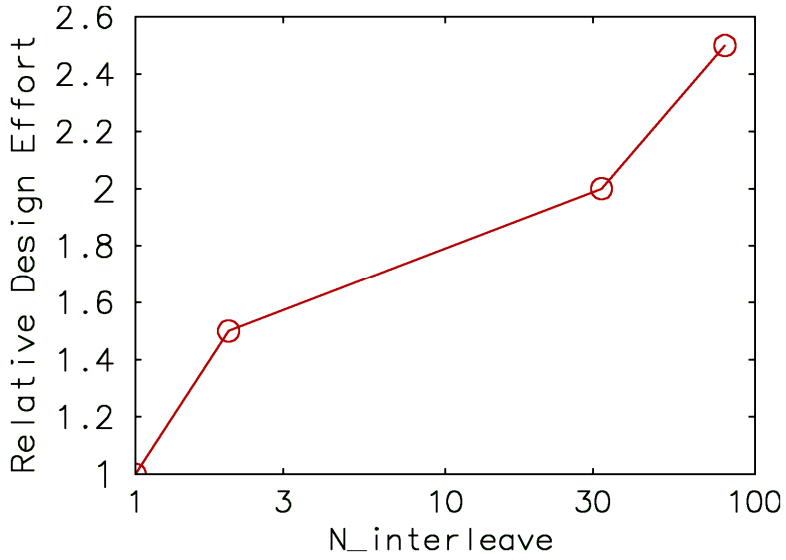
Overhead Factors for Interleaved ADCs

- Power:
  - Power in ADC slices can be a fraction of total ADC power
  - Example: 32-way, 4-GSa/s ADC

32 ADC slices	1.6 W	38%
Samplers + clocks	0.9 W	21%
Multiplexors and outputs	1.7 W	41%
Total	4.2 W	

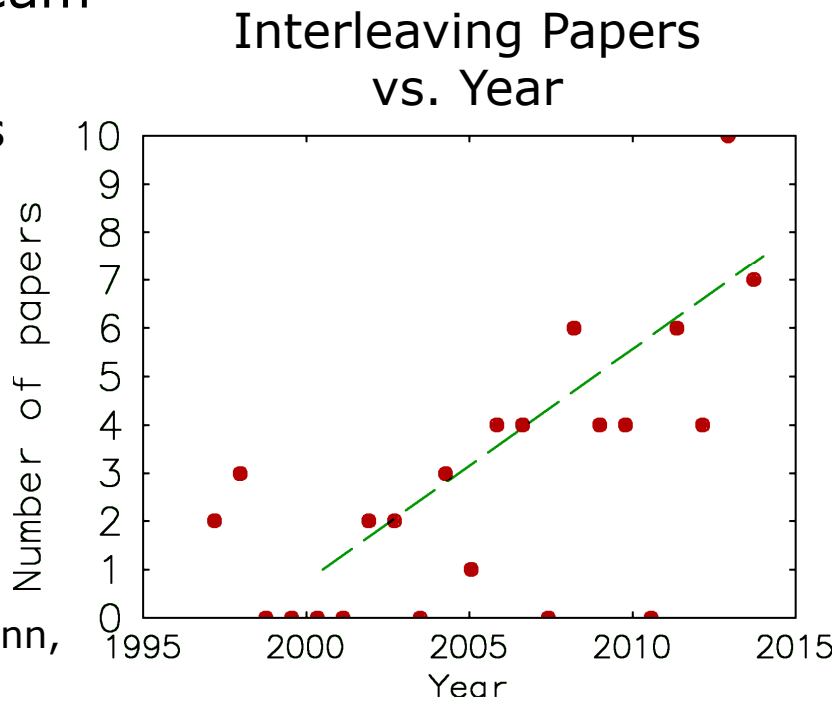
- Design Overhead:
  - More optimization variables
  - More circuits that interact
  - More clocks
  - V_{IN} and clock distribution
  - Data collection and multiplexing
  - Calibration
  - Optional: Memory and/or DSP

Historical Data:
Relative Design Time vs. Interleave Factor



Interleaved ADC Trends

- Much more power-efficient core slices
  - Power-Efficiency FOM has dropped by ~10x since 2002
  - Use of interleaving has propelled SARs to prominence
- More background cal
  - Making the transition from academia to industry
- Interleaving has become mainstream
  - Lots of papers at ISSCC
  - Massive interleaving for 12+ Gb/s wireline link products
  - Becoming "just another ADC topology"



"ADC Performance Survey 1997-2014", B. Murmann, web.stanford.edu/~murmann/adcsurvey.html

The Future for Interleaved ADCs

- When will all ADCs be interleaved?

  Never!

  - Design complexity
  - Overhead for power and design time

- The Skyrocketing Price of Moore's Law
  - Interleaving decouples process choice from sample rate requirements

Acknowledgments

- John Corcoran
- Tom Hornak
- Robert Neff
- ~50 other past and present members of HP/Agilent/Keysight who designed the chips described here

- Brad Doerr
- Lon Hintze
- Dennis Weller
- Mike Beyers

(END)

References

"A 100 Ms/s Waveform Digitizer with Comprehensive Error Correction", John Corcoran, Tom Hornak, Workshop of High Speed A/D Conversion, Feb 11, 1980

"Time interleaved converter arrays", Black, W., Jr. ; Hodges, D., ISSCC 1980 and JSSC 1980

"A 1 GHz 6-bit ADC System", Ken Poulton, John J. Corcoran, Thomas Hornak, IEEE Journal of Solid State Circuits, Dec 1987

"A 6-bit, 4 GSa/s ADC Fabricated in a GaAs HBT Process", Ken Poulton, Knud L. Knudsen and John J. Corcoran Keh-Chung Wang, Randall Nubling, Richard Pierson, Mau-Chung F. Chang and R.T. Huang, 1994 GaAs IC Symposium, Oct 1994

"A 6-bit, 4 GSa/s GaAs HBT ADC", Ken Poulton, Knud L. Knudsen, John J. Corcoran, Keh-Chung Wang, Randy Nubling, Richard Pierson, Mau-Chung F. Chang, Peter Asbeck and R.T. Huang, IEEE Journal of Solid State Circuits, Oct 1995

US 4,271,488 "High-Speed Acquisition System Employing an Analog Memory Matrix"

"Investigation of an Analog Sampling and Storage Chip", HP internal report, ca. 1995

"Baseband Vector Signal Analyzer Hardware Design", Manfred Bartz, Keith A. Bayern, Joseph R. Diederichs, and David F. Kelley, HP Journal, Dec 1993, pp 31-39 First known use of BG cal (to cancel dither)

"An 8-GSa/s 8-bit ADC System", Ken Poulton, Knud L. Knudsen, John Kerley, James Kang, Jon Tani, Eldon Cornish and Michael VanGrouw, IEEE VLSI Symposium on Circuits, 1997

"A 4-GSample/s 8b ADC in 0.35-um CMOS", Ken Poulton, Robert Neff, Art Muto, Wei Liu, Andy Burstein, Mehrdad Heshami, ISSCC, pp 166-167, Feb 2002

"A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration", Shafiq Jamal, et al, JSSC, Dec 2002, pp1618-1627

References 2

"A 20 GS/s 8 b ADC with a 1 MB memory in 0.18-um CMOS", Ken Poulton, Robert Neff, Brian Setterberg, Bernd Wuppermann, Tom Kopley, Robert Jewett, Jorge Pernillo, Charles Tan, Allen Montijo, ISSCC, pp 318-319, Feb 2003

"Analog-to-Digital Converters- 20 Years of Progress in Agilent Oscilloscopes" , John Corcoran and Ken Poulton, Agilent Measurement Journal, vol. 1, pp 34-40, March 2007

Robert Neff, "Clock Challenges for GHz ADCs", Clock Synthesis Design Forum, ISSCC 2010

"A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction", Setterberg, B.; Poulton, K.; Ray, S.; Huber, D.J.; Abramzon, V.; Steinbach, G.; Keane, J.P.; Wupperman,B.; Clayson, M.; Martin, M.; Pasha, R.; Peeters, E.; Jacobs, A.; Demarsin, F.; Al-Adnani, A.; Brandt, P. , ISSCC 2013

"A 10-b 120-Msample/s Time-Interleaved Analog-to-Digital Converter With Digital Background Calibration", Shariq Jamal, et al, JSSC, Dec 2002 pp1618-1627 – first background correction of timing errors

S. M. Jamal, D. Fu, M. P. Singh, P. J. Hurst, and S. H. Lewis, "Calibration of sample-time error in a two-channel time-interleaved analog-to digital converter," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 1, pp. 130–139, Jan. 2004

"ADC Performance Survey 1997-2014", B. Murman, web.stanford.edu/~murmann/adcsurvey.html

"Technologies for Very High Bandwidth real-time Oscilloscopes", Pupalaikis, et al, lecroy.com

"A Polynomial-Based Time-Varying Filter Structure for the Compensation of Frequency-Response Mismatch Errors in Time-Interleaved ADCs", Johansson, IEEE Signal Processing, 2009

References – Frequency Interleaving

"High speed A/D Conversion using QMF banks", A Petraglia, S.K. Mitra, ISSCC 1990

"System for converting a signal between continuous-time and discrete-time", US 5568142, Velazquez, Nguyen, Broadstone, Oct 1994

"Design of hybrid filter banks for analog/digital conversion," S. R. Velazquez, T. Q. Nguyen, and S. R. Broadstone, IEEE Trans. Signal Process., vol. 46, no. 4, pp. 956–967, Apr. 1998.

"High bandwidth real-time oscilloscope", US 7058548, Peter J. Pupalaikis, David C. Graef, Jun 2006

S. Jalali Mazlouman and S. Mirabbasi, "A Frequency-Translating Hybrid Architecture for Wideband Analog-to-Digital Converters," IEEE Transactions on Circuits and Systems II, vol. 54, no. 7, July 2007, pp. 576-580 – multiple I-Q mixers

"Techniques for Extending Real-Time Oscilloscope Bandwidth", tek.com, 2013

"Test and measurement instrument including asynchronous time-interleaved digitizer using harmonic mixing", US 8742749, Jun 2014

"Method of crossover region phase correction when summing signals in multiple frequency bands", US 7711510, Pupalaikis, et al, May 2010

"Calibrating reconstructed signal using multi-tone calibration signal", US 8849602, Ken Nishimura, Ken Rush, Oct 2014

S. Jalali Mazlouman, S. Sheikhaei, and S. Mirabbasi, "Digital Compensation Techniques for Frequency-Translating Hybrid Analog-to-Digital Converters," IEEE Tran. on Instrumentation and Measurement, vol. 60, no. 3, pp. 758-767, March 2011.