26.3 A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction

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Metastable events in ADC comparators cause large errors that cannot be tolerated in test and measurement applications that record data over extended time intervals. This work utilizes BiCMOS technology to provide high dynamic range analog to digital conversion at 2.5GS/s with a metastable error rate of less than one error per year and better than 78dB SFDR over a 1GHz BW.

The metastability error rate goal motivated the ADC architecture shown in Fig. 26.3.1. Comparator regeneration time constants in the 130nm BiCMOS process are too slow to meet the target error rate at a 2.5 GHz clock speed. Accordingly, eight 312.5MS/s ADC slices were interleaved to achieve the aggregate 2.5GS/s with an error probability of less than 10^{-17}.

To avoid SNR degradation due to jitter, sampling time errors must be less than 90fs rms. This accuracy is achieved through a combination of a low noise clock path and a 2-rank T/H architecture, as shown in Fig. 26.3.1. Clocked at the full 2.5GHz sampling rate via a low-jitter CMOS driver chain, the first T/H stage sets the sampling instant. Eight time-interleaved second-rank T/H stages subsequently sample the output of the first-rank T/H. Because the first T/H stage determines the sampling instant, random jitter from the clock divider and second-rank T/H sampling do not contribute to interleaving errors. The measured sampling time error of the ADC is less than 70fs rms.

The first stage of each of the 8 pipelined ADCs resolves 3 bits plus redundancy using a 15-level flash ADC and DAC. The first stage's residue amplifier contains a transconductor that transforms the voltage residue into a current for further conversion with 15 radix-1.7 current-mode stages [1]. Analog inter-stage gain errors are corrected in an on-chip digital radix converter whose coefficients are continuously updated from an on-chip background calibration engine. Sufficient redundancy is provided throughout the analog signal path to perform all corrections digitally.

Mismatches in the 14 equally-weighted first stage DAC elements are detected by permuting the connections between the comparators and the DAC elements with permutation logic controlled by a pseudo-random code. The permutation allows the LMS calibration loops to measure and digitally correct DAC element weight mismatches [2]. To ensure that the calibration loops always see permuting activity with input signals near plus or minus full scale, two additional DAC elements and permuter inputs are included. A static logic '1' and '0' are permuted along with the 14 comparator outputs.

Achieving 14-bit performance requires calibration of the first 11 stages of the pipelined ADC. The comparator thresholds in each stage are pseudo-randomly dithered. One LMS calibration loop per stage minimizes the correlation of this dither with the output code to determine the correct stage weight [3].

To avoid interleaving artifacts, additional calibration loops align the gain and offset of each of the eight ADC slices. These slice-to-slice gain and offset calibrations are facilitated by perturbing the analog signal path with pseudo-random stimuli. For gain calibration, an analog dither signal is injected into the signal path between the first- and second-rank T/H as shown in Fig. 26.3.2. Fig. 26.3.2 also shows how the signal path is pseudo-randomly chopped for offset calibration. Diode-connected load transistors M3 and M4 provide first-order linearization for differential pair M1 and M2. Resistors R1 and R2 allow M3 and M4 to serve a second purpose as source followers to inject the dither. BJTs Q1–Q4 perform the chopping operation, inverting the output signal polarity in response to the chop PRBS. BUF1 and BUF2 modulate the chop drive signal at the bases of Q1–Q4 with a level-shifted version of the input signal. This bootstrapping ensures that M1 and M2 have a reasonably constant Vgd for improved linearity and reduced thermal transients.

The analog dither serves as an amplitude reference for all slices. The LMS gain calibration loops detect any correlation of the output code with the pseudo-random dither after the dither sequence has been subtracted. Slice-to-slice gain calibration is achieved when the gain calibration loops have adjusted all of the slice gain coefficients to minimize any residual dither [4].

The chopper enables an offset calibration that correctly converges in the presence of any ADC input signal. Because the chopper is driven with a zero-mean PRBS, calibration is achieved when the offset calibration loops converge to coefficients that produce a slice digital output that also has zero mean [5].

When the chop polarity changes, transistors M3 and M4 in Fig. 26.3.2 experience a large change in Vds that causes the device power dissipation to change. The resulting device temperature change is significant enough to introduce a 0.1% PRBS-modulated thermal transient that would degrade the SNR by 6dB if left uncorrected. An on-chip digital filter corrects this chopper-induced thermal artifact (Fig. 26.3.1). The impulse response of the transient is measured with on-chip correlation hardware in a foreground self-calibration step. Because the slow thermal transients require a large 32-tap filter for correction, a poly-phase fast FIR architecture was chosen to reduce the required filter gate count.

The digital dynamic linearity corrector (DLC) shown in Fig. 26.3.3 improves second- and third-order dynamic harmonic distortion. Using a slope estimation FIR filter to estimate the derivative of the input signal, the DLC computes several second- and third-order products of the signal and its derivative to compute dynamic linearity corrections [6]. As shown in Fig. 26.3.4, the DLC provides an SFDR improvement of more than 8dB for input signals between 200MHz and 1GHz.

Integrating all of these elements for high speed, high dynamic range and low bit error rate comes at the cost of high complexity and high power dissipation. Total power dissipation is 23.9W: 2.5W for the 2-rank T/H, 1.8W for clock distribution, 13.1W for the 8 ADC slices, 2.6W for the digital signal path and DSP, 2.7W for background calibration and 1.2W for the dual parallel output data ports. The SFDR is 78dB for input signals from DC to 1GHz with a -1dBFS input. As shown in Fig. 26.3.5, INL is ±1.5LSB, limited by third harmonic distortion. The power spectrum in Fig. 26.3.6 demonstrates the effectiveness of the 224 continuously-operating background calibration loops that reduce interleaving spurs to below -82dBc. The background calibrations converge with all loops operating simultaneously with arbitrary inputs to the ADC. The 61dB SNR is maintained for signals up to 1GHz due to the low 70fs rms jitter.

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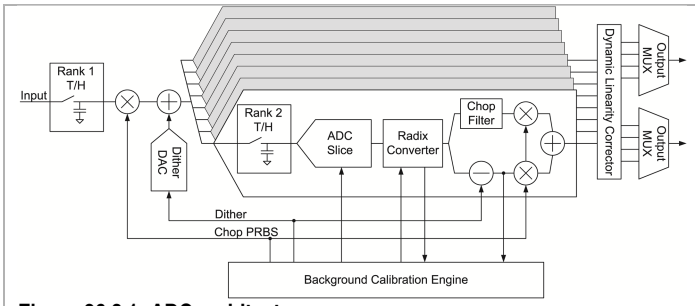

Figure 26.3.1: ADC architecture.

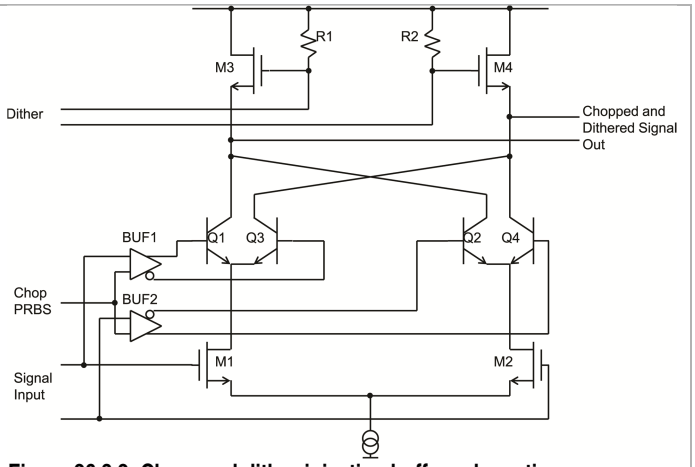

Figure 26.3.2: Chop- and dither-injection buffer schematic.

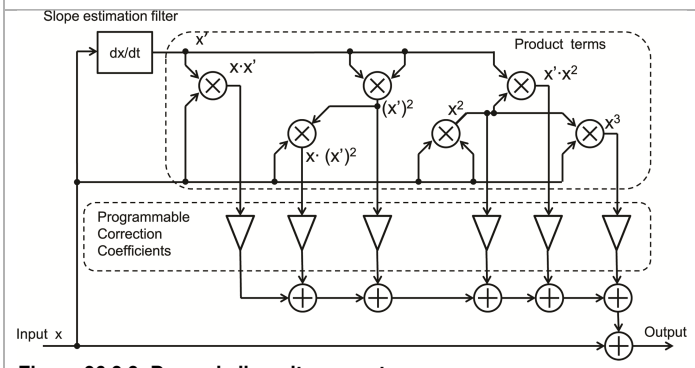

Figure 26.3.3: Dynamic linearity corrector.

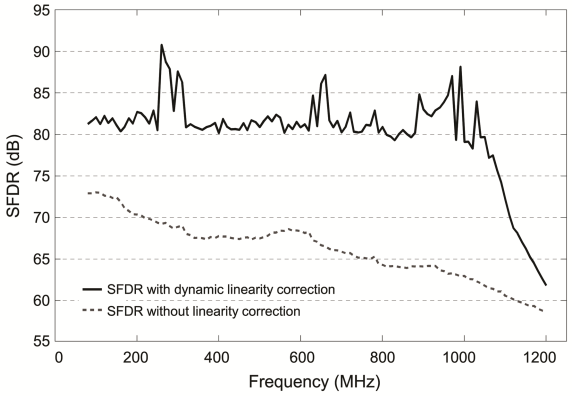

Figure 26.3.4: SFDR vs. frequency with a -1dBFS input.

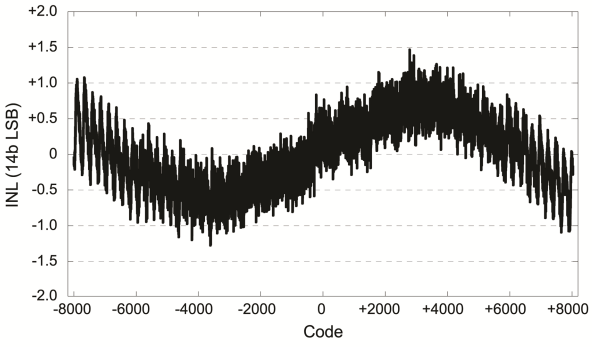

Figure 26.3.5: Integral nonlinearity.

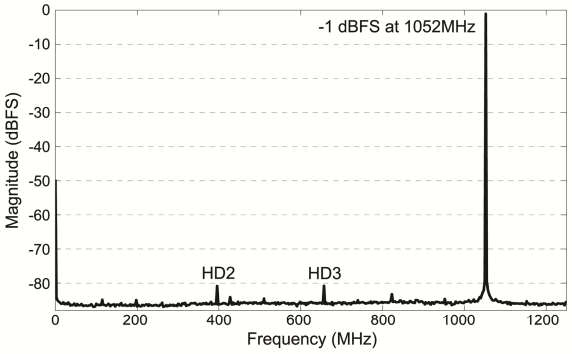

Figure 26.3.6: Welch power spectrum of 256 1024-point FFTs.