

A 7.2 GSa/s, 14 bit or 12 GSa/s, 12 bit Signal Generator on a Chip in a 165 GHz f_T BiCMOS Process

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***Abstract* – We present a complete signal generator with integrated digital-to-analog convertor (DAC) on a chip which can generate complex waveforms at up to 7.2 GSa/s with 14 bit resolution or at up to 12 GSa/s with 12 bit resolution. The 3 dB bandwidth is 4.4 GHz. The chip includes digital signal processing (DSP) logic for agile generation of wideband modulated RF signals (up to 480 MHz modulation bandwidth) as well as high fidelity chirp and continuous wave signals. There is also DSP for integral non-linearity error reduction and suppression of clock sub-harmonics. The DAC uses a segmented architecture with 4 unary most significant bits and an R/2R ladder for the 10 binary least significant bits. Distributed resampling is applied to all current sources to improve the dynamic performance. At 7.2 GSa/s it delivers at least 67 dB spurious free dynamic range (SFDR) across the whole Nyquist region and an SNR of 62 dB. It demonstrates -157 dBc/Hz phase noise at 10 kHz offset from a 1 GHz carrier, 22 dB better than known**

synthesized signal generation instruments. The chip is built in a 165 GHz f_T , 130 nm BiCMOS process and is packaged in a 780 ball BGA.

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***Index Terms:* Digital-to-analog conversion (DAC), direct digital synthesis (DDS), phase noise, spurious free dynamic range (SFDR).**

I. INTRODUCTION

High-speed, high-resolution digital-to-analog converters (DACs) can greatly simplify RF signal generation systems for cellular communication, wireless networking, radar, and instrumentation applications. With a fast enough DAC, RF signals with wideband complex modulation can be generated directly with no need for phase-locked loops, frequency multipliers, or upconverting mixers. In addition, the frequency switching speed of such a DAC-based source can be orders of magnitude faster than sources based on traditional block diagrams. Finally, close-in phase noise can be extremely low.

We report a 7.2 GSa/s, 14 bit BiCMOS DAC [1] that operates with at least 67 dB spurious free dynamic range (SFDR) over the whole Nyquist region. We believe this is better

performance than any previously reported DAC [2] over this frequency range. The DAC can also operate at 12 GSa/s with 12 bit resolution.

The chip incorporates over 5 million gates of digital signal processing (DSP) logic for signal generation, baseband interpolation and agile modulation. There is also DSP logic for integral non-linearity (INL) error reduction and suppression of sub-harmonics of the clock.

Fig. 1 shows the full chip block diagram. The DSP logic is implemented in 0.13 μm CMOS standard cells. The high-speed multiplexer (MUX) is implemented in custom CMOS and bipolar current mode logic (CML). The DAC itself is implemented primarily with 165 GHz f_T bipolar devices.

II. DIGITAL-TO-ANALOG CONVERTER

A. Block Diagram

The DAC uses a segmented architecture with 16 equal most-significant-bit (MSB) current sources and binary-weighted least-significant-bit (LSB) current sources. The MSBs account for 4 bits of resolution while the LSBs give an additional 8 or 10 bits depending on the operating mode. One additional redundant LSB (RLSB, described later) is used for current source error correction and is denoted as “+1” in the LSB count.

Fig. 2 shows the simplified block diagram of the DAC portion of the chip. (Although shown as single-ended, all of the signals are differential pairs.) The DAC consists of two sub-DACs (A and B). The latches receive the 27 data bits from the high-speed multiplexer. The latch outputs control the current switches to direct each current source towards the V_{out+} or V_{out-} output. Those currents are resampled [2,3] by switches driven with Clk to select settled half-cycles of

current, producing a return-to-zero (RZ) waveform from each sub-DAC. The per-current-source resampling achieves the cleanest possible output current pulses but the RZ waveform is unacceptable in many applications. This is solved by delaying sub-DAC B data by a half-cycle of *Clk* so that its current pulses can fill in the half-cycles that are missing due to the resampling in sub-DAC A, giving a non-return-to-zero (NRZ) final waveform [4]. Resampling could be accomplished with a single switch [5], but it is impractical to make such a switch linear to 70 dB at high sample rates. This is because the speed of the switch varies with the signal current passing through it. The distributed resampling used here [2] has better linearity because each resampling switch is resampling a current which is either on or off.

The LSB currents are scaled by the R/2R ladder while the MSB currents are applied directly to the output nodes. Coupled inductors at the chip outputs partly compensate for the output capacitance of the current sources and equalize the rise and fall times of the outputs. The 54 unit current sources are scaled by the two reference voltages $VREFA$ and $VREFB$ to allow gain control. An RZ output waveform can be achieved by turning off one set of current sources with the corresponding $VREF$. This provides better gain flatness across Nyquist but 6 dB less power at low frequencies.

The decision to choose a partition of 16 MSBs and 10 LSBs was a tradeoff between better inherent linearity and the rapid increase in power when the number of MSBs is increased. Higher-order nonlinearities are mostly due to mismatch in gain and timing of the MSB and LSB sections and these become smaller as the LSBs are reduced in magnitude.

B. Clock Circuits

The major problems in the design of the clock circuitry were maintaining low phase noise and ensuring correct time alignment between the data latches and the resampling switches. The differential input clock is received on $25\ \Omega$ lines and terminated on-chip. This impedance allows use of a clock balun with $50\ \Omega$ differential output impedance. The nominal input clock power is +7 dBm to keep the thermal noise floor below the noise floor needed for the goal of -160 dBc/Hz for the broad-band floor of a 3 GHz output signal. The total jitter budget for the clock was 30 fs RMS. Six stages of scaled ECL buffers consuming a total of 1 W drive the final stage which swings 300 mV across $3\ \Omega$ resistive loads. This drives a 32-way binary clock tree to achieve simultaneous resampling of all 27 currents. The extra 5 branches are terminated in dummy circuits at the edges of the current source array.

The *Clk* input drives two clock paths: one to the resampling clock and one to everything else. In order to achieve proper alignment of resampling relative to data timing in spite of different loading and clock paths, an on-chip delay circuit in the second clock path allows adjustment in 64 steps of 1.5 ps. This is implemented with ECL gate delays for the major steps and capacitive loading for the minor steps. A single delay setting was found to work well for all tested circuits.

The resampling clock can be forced low so that only Sub-DAC A is used; this enables operation as an NRZ DAC without resampling. This mode has fewer switching transients and produces smoother waveforms for time-domain applications. It has somewhat higher jitter and up to 12 dB more harmonic distortion than the resampled NRZ mode.

C. Unit Current Source And Switches

A simplified diagram of the unit current source and switches is shown in Fig. 3. Beginning at the bottom, the current (nominally 2 mA) is determined by V_{REF} and V_{B1} , which is biased one diode-drop above the substrate voltage of -3.3 V. The data switches direct the current towards the plus or minus output. The current is resampled by Clk and sent through cascodes biased by V_{B2} to the output. All of the current sources in the DAC are identical and differ only in where their outputs are directed. In the case of the LSBs, the currents go to a node in the R/2R ladder while the MSBs go directly to the outputs. The output common mode voltage is set by V_{CCA} which provides a clean reference as it is used for nothing else.

Inter-symbol interference (ISI) or memory effects in the sources were addressed at three levels. Capacitance at the emitters of the data pair was kept as low as possible. The maximum impedance at the emitters of the resampling pairs was limited by sharing a small amount of current through “trickle resistor” R_T between the two nodes. The voltage across this resistor will be determined by the logarithmic V_{BE} I-V characteristic and will be quite stable over a wide range of operating current. The value was chosen to reduce the impedance enough to get good reduction of the ISI without taking too large a part of the signal current to the complement output. This method was chosen for its simplicity and relatively small parasitics. Finally, the emitters of the cascode devices have a small, fixed current to similarly reduce their maximum impedance. The two trickle currents amount to about 15% of the nominal DAC current.

In this design, V_{BE} mismatch in the resampling pair can cause INL. If the “pass” device turns on at a lower voltage than the “dump” device, the output current pulse will be wider than expected and the average output current for that source will be larger than nominal even though

the static current may be correct. Since each current pulse is only about 60 ps wide, and each MSB current source has a nominal weight of 1024 LSBs, even sub-picosecond changes in the pulse width can cause a significant mismatch. The INL is as large as ± 6 LSBs which if left uncorrected would cause spurious outputs far larger than the design goal. Two methods of suppressing spurious are discussed in the next sections: Current Source Error Correction (CSEC), and Thermometer Encoding with Dynamic Element Matching (DEM) [6].

The 165 GHz f_T devices used contribute to the speed and performance of the current sources and the complete DAC in several major ways. First, the maximum speed of the final digital drivers is enabled by the raw speed of the devices and even so the design is well up the speed-power curve for this process. The devices allowed good gain in the clock path without inductive tuning to give fast switching and low phase noise. Finally the high gain of the NPNs assures fast switching and low mismatch in the resampling pairs which minimizes sample-rate dependent mismatch.

III. DIGITAL SIGNAL PROCESSING

A. Introduction

Fig. 4 shows the digital circuits that precede the MUX and DAC. These are implemented in CMOS standard cells using a synthesis design flow. Datapath configuration supports three main modes of operation, all of which can take advantage of error correction functions (distortion and sub-harmonic suppression):

- in *Direct* mode the full DAC data stream comes in the Data Port. This mode provides the greatest usable signal bandwidth but places more burden on parts external to the chip. For sample rates above 7.2 GSa/s only direct mode is supported.
- in *Direct Digital Synthesis* (DDS) mode, sine waves are generated by the two on-chip numerically controlled oscillators (NCOs). This supports continuous wave (CW), chirp sweep and angle-modulated frequency-synthesis applications. The two NCOs operate independently.
- *Interpolated* mode allows the user to supply a lower-sample-rate complex baseband or IF signal which is up-sampled and filtered to the full DAC sample rate to modulate NCO-generated signals.

Since it is relatively inexpensive to reduce digital noise compared to analog and mismatch noise, the digital functions are designed for a total quantization noise spectral density of less than -171 dBc/Hz in a 7.2GSa/s system. This is 5-10 dB below the analog noise level depending on the intended signal frequency F_{OUT} and corresponds to a signal-to-noise ratio (SNR) of 75.4 dB

B. High-speed Multiplexer

The MUX takes data from the DSP circuits at a maximum rate of 300MHz (depending on mode and sample rate) and sends it across the isolation region (discussed below) to the DAC at up to 8GSa/s in single words. For higher sample rates, a second set of lines is activated so that 12GSa/s is achieved with only 6GHz data rates. This requires a second MUX on the DAC side for the double-data-rate mode which is switched in only for that mode. The first part of the MUX is implemented in standard CMOS up to rates of 1.2 Gb/s/wire, then bipolar CML and ECL circuits achieve the final sample rate. The clocking has a reverse path; starting from the DAC

side the full rate clock signal Clk is divided down first by bipolar and then by CMOS circuits with a factor of 24, 32 or 48 (depending on the mode and sample rate) to generate the digital core clock ($CClk$) for the DSP section.

C. Data Port

Input data samples and modulation parameters enter the chip via the 153 bit double data rate (DDR) Data Port at up to 1 Gb/s per pair. Time alignment of the signals is secured via self-calibrated per-channel delays and channel bonding. Configurability allows reallocation of input bits to trade off input data sample rate, data word widths, and modulation parameter update rate.

D. Interpolation

The interpolation filters provide 90 dB image rejection and 1 dB passband flatness. Interpolation ratios of 12, 24 and 48 are possible, with available signal bandwidth of 480 MHz, 240 MHz and 120 MHz respectively. In the latter mode (interpolation ratio of 48), two distinct signals can be interpolated concurrently. The interpolator is designed as a sequence of interpolation stages for which a polyphase implementation is used. Depending on the interpolation ratio chosen, every stage computes one or more samples per $CClk$ cycle. Every cycle, the last active stage computes 24 complex samples (one for each polyphase component) of the underlying full DAC rate (F_s) signal.

Signal-dependent supply noise and temperature variation in the DSP is a source for spurious signals at the DAC output. Fig.5 shows how this was minimized in the interpolator. A pseudorandom source (designated PRBS) generates a 1 bit signal that is scaled by 2^K (to fullscale of the *Input* signal) and added to the *Input* signal. Two interpolators with identical transfer functions then process the signals S_0 and S_1 into T_0 and T_1 respectively. Note that the auxiliary

interpolator has a very small power and area cost, since its datapath is only 1 bit wide. The interpolators are purely linear, i.e. there is no signal quantization (rounding or clipping) inside, so the *Output* (equal to $T_0 - T_1$) is exactly the interpolated *Input* signal. Therefore the interpolation function is unchanged, but the digital activity level is always 50%, independent of the input signal.

E. Signal Generation and Modulation

The chip contains two NCOs that can be operated independently. A simplified NCO block diagram is shown in Fig. 6. The instantaneous frequency f_{inst} is determined by programmable parameters: center frequency (f_c), frequency (f_M) or phase (p_M) modulation word, maximum FM or PM deviation (M) and frequency sweep rate (f_{SW}). Only one of f_M and p_M can be non-zero. For phase calibration of the signal path, a phase offset θ is added to the accumulated f_{inst} , resulting in the phase signal φ . Both f_{inst} and φ have 72 bit resolution. The phase interpolator computes a polyphase component vector $\Phi_{24 \times 1}$ of the interpolated phase, which drives an array of 24 phase-to-amplitude converters (PACs) to produce the complex polyphase components vector $C_{24 \times 1}$ of the full DAC rate underlying signal.

Two frequency switching modes are supported. In phase-continuous switching (Fig. 7 upper) the phase slope is changed in a single *CCLK* cycle with no jump in the phase or the resulting voltage waveform. In phase-repeatable switching (Fig. 7 lower) the instantaneous frequency changes from f_1 to f_2 and back to f_1 , but the phase can be jumped back to the original phase trajectory for f_1 .

In interpolated mode, the $C_{24,1}$ signal in Fig. 6 is amplitude modulated with the complex interpolator output signal *Interpolated*; in DDS mode it is multiplied by the programmable value

Amplitude. Only the real component is computed. Any subset of modulation parameters ($f_c, f_{sw}, f_M, p_M, M, \theta, Amplitude$) can change with time accuracy of one $CCLK$ clock cycle.

Up to 36 bits of the input Data Port can be allocated to change the modulation parameters without interrupting the baseband I/Q data flow. This allows any two parameters (e.g., frequency and amplitude) to be updated each $CCLK$ cycle, as often as every 3.3 ns. The result is an agile signal source that supports CW, chirp sweep, and amplitude, phase and frequency-modulated signals.

F. Sub-Harmonic Filtering

The digital logic is clocked at a rate (F_{CCLK}) which is an integer sub-multiple (24, 32 or 48) of the DAC clock rate. This can generate spurious signal components (“sub-harmonics”) in the DAC output at frequencies F_{spur} , see (1).

$$F_{spur} = m \cdot F_{OUT} + n \cdot F_{CCLK}, \quad \text{for } m = 0 \text{ or } 1; n \in \mathbb{Z}. \quad (1)$$

The sub-harmonic filter (SHF in Fig. 4) includes a programmable 9 tap linear periodic time variant FIR filter. The time periodicity can be programmed for the different sub-multiple factors (24, 32 or 48). This filter can suppress sub-harmonic spurs of the form $F_{spur} = F_{OUT} + n \cdot F_{CCLK}$. It is implemented as an incremental filter with a power of 2 block scaling with respect to the direct path, see (2).

$$y(n) = x(n-4) + 2^{-K} \sum_{k=0}^8 h_{n \bmod N}(k) x(n-k), \quad \text{for } K = 4, \dots, 16. \quad (2)$$

A periodic offset can be added to the signal as a pre-compensation for sub-harmonic spurs the form $F_{spur} = n \cdot F_{CLK}$. This offset has sub-LSB resolution and a range equal to the full DAC amplitude. This allows an alternative use as a 24-48 sample memory to play short waveforms.

G. Thermometer Encoding with Dynamic Element Matching

The four MSBs of the binary signal are converted into a 16 bit unit-weighted thermometer code. In addition, a redundant representation using a redundant current source (RLSB) with a weight of 128 LSBs is introduced to allow processing headroom for the subsequent current source error correction. The optional dynamic element matching [6] (DEM) pseudo-randomly permutes the 16 thermometer-encoded MSBs with white, unshaped noise signals. Linearity errors due to current source mismatch are scrambled into pseudo-random whitened noise, thereby trading improved SFDR for degraded noise floor.

H. Current Source Error Correction

The CSEC applies pre-distortion to the digital signal to mitigate current source mismatches. This reduces the harmonics when no DEM is used or lowers the noise floor when DEM is used.

The CSEC corrects two types of current source random mismatch errors: DC amplitude errors and pulse width errors. The errors in the two sub-DACs are independent, but we can treat them as mean errors (the average of a given current source in the two sub-DACs) and difference errors. Corrections for mean and difference errors are mapped to respective base filter responses $B_j(z)$ with $j=0,1$. The filter for mean errors is a unit pulse as seen in Fig 8. The coefficient H_{00} is set to the time×voltage area of the error for that current source, to provide correction of both pulse height errors and pulse width errors. The difference error shape is a positive half period followed by a negative half period, which cannot be exactly corrected with predistortion data

(full period pulses). The filter for the difference errors is anti-symmetric with coefficients 1, -2, 5, -8, 0, 8, -5, 2, -1 (each divided by 32). This approximates the spectrum of the difference error impulse response to within 2 dB out to 80% of the Nyquist frequency, allowing approximately 12 dB suppression of difference errors.

There are 19 *correctable* current sources: the 16 MSBs (S_{18}, \dots, S_3) and the 3 largest LSBs (S_2, \dots, S_0). The other LSBs and the RLSB (introduced in the thermometer encoder) are considered *correction* current sources that can absorb correction terms for the correctable current sources. For each correctable current source S_i (with $i=0..18$), a programmable value H_{ij} weights the degree of correction needed for each of the two error types ($j=0,1$). Values for H_{ij} are found by a foreground calibration procedure and stored on chip. The total current source error correction for current source S_i is shown in (3) and Fig. 8.

$$C_i(z) = S_i \sum_{j=0}^1 H_{ij} B_j(z). \quad (3)$$

The CSEC output is the sum of the total correction $C(z)$, shown in (4), and the input signal of the CSEC.

$$C(z) = \sum_{i=0}^{18} C_i(z). \quad (4)$$

The redundant current source (RLSB) has a weight of 128 LSBs, which provides a correction range for $C(z)$ of ± 64 LSBs. Provided that $C(z)$ does not exceed this range, the sum of the CSEC input *correction* current sources and $C(z)$ will not generate a carry into the *correctable* current sources (which would call for a different value of $C(z)$).

Systematic ratio error between the MSB and LSB currents is often a major source of INL in segmented DACs. The CSEC is also used to correct this error.

IV. ANALOG/DIGITAL ISOLATION MEASURES

Because of the aggressive goals for SFDR (clock sub-harmonics below -90 dBc), many methods are used to reduce cross-talk from the digital side to the analog side.

The first technique is physical separation of the two parts by an isolation region 1.5 mm wide. This is visible on the chip die photo (Fig. 9). The isolation region is further divided into six vertical stripes each 250 μm wide with separate substrate connections for each stripe with those connections remaining separate all the way out of the package. Each stripe provides about 6 dB of attenuation. A low-doped-substrate process is necessary for this to work.

The supplies, including ground, are kept separate out to the package pins. Both NMOS and PMOS devices in the digital circuits are isolated from the substrate with a buried n+ isolation layer.

Sub-harmonic spurs, including mixing of sub-harmonics with the signal, were measured at less than -95 dBm. Compared to the total aggressor clock power (+33 dBm for F_{Ck} at 300 MHz) this shows a power-ratio isolation of 128 dB. This isolation is effective enough that activity randomization in the interpolator and the sub-harmonic filter are not required and are turned off to save power.

V. MEASUREMENTS

A. Test Setup

The packaged chip is mounted on a characterization board, either soldered or in a socket. The board includes an FPGA that can exercise all the modes of the chip. The FPGA includes 64K samples of arbitrary waveform memory. The differential output of the DAC is converted to single-ended with a balun. The following tests were done in NRZ mode with DEM on and calibration off unless otherwise stated.

B. Results

The INL of the DAC is shown in Fig. 10. Without (CSEC) calibration or DEM, the INL is ± 6 LSBs, mostly due to pulse-width mismatch among the distributed resampling pairs, and the noise floor is -161 dBc/Hz. With DEM on, we reduce the INL to ± 2.3 LSBs, but the noise floor rises to -158 dBc/Hz since the MSB INL has been converted to noise. A repeating pattern due to LSB mismatch remains. If we instead turn on the CSEC calibration, we reduce the INL to ± 1.2 LSB, suppress the errors due to the LSBs and recover the noise floor to -160 dBc/Hz. The broadband noise floor of -161 dBc/Hz at 3 GHz output confirms that the circuit has 30 fs rms thermal jitter.

Fig. 11 shows a spectrum of the DAC output with F_{OUT} at about 2.2 GHz and F_S at 7.2 GSa/s. When computing SFDR, we include all spurs from DC to the Nyquist frequency, including the harmonics of the intended tone. For all F_{OUT} the SFDR is dominated by the (direct or folded) second or third harmonic: $2 * F_{OUT}$, $F_S - 2 * F_{OUT}$, $3 * F_{OUT}$ or $F_S - 3 * F_{OUT}$.

Fig. 12 shows how SFDR varies with F_{OUT} . At F_S of 7.2 GSa/s, we achieve 67 dB SFDR across the whole first Nyquist region (DC to $F_S/2$). At F_S of 12 GSa/s, we achieve 55 dB SFDR. SFDR gets worse at higher clock rates as the current switch nodes get less settling time.

Fig. 13 shows how SFDR varies with clock rate F_S . At each point we plot the worst SFDR for any F_{OUT} from DC to $F_S/2$ at that sample rate. The chip actually operates up to 13.6 GSa/s. DEM improves SFDR by about 6 dB for clock rates above 6 GSa/s because it averages out any mismatch errors among the MSB current sources.

Fig. 14 shows the SFDR (across the whole Nyquist band) of this DAC compared to other gigasample-per-sample DACs from publications and data sheets [2],[7]-[16]. At any DAC data rate F_S from 1 to 12 GSa/s, this DAC achieves at least 14 dB better SFDR than the others. This is due primarily to the use of fast bipolar devices in the high-speed flipflops and the DAC current switches, a single-core DAC (no time interleaving), distributed resampling, and a segmented architecture with dynamic element matching.

Close-in phase noise of the DAC is quite low because of the use of resampling and an all-bipolar signal path from the clock input to the resampling devices to the analog output. To distinguish the phase noise of the DAC from the clock source, we drive two chips from a single low-noise dielectric resonator oscillator (DRO) clock source. The chips are set to the same F_{OUT} with DEM off. The DAC outputs are each converted from differential to single-ended with baluns and the two single-ended outputs are subtracted using a third balun. This cancels clock-related noise so it does not appear in the output. We then reduce the dynamic range to be measured by adjusting the phase of the two DACs to cause partial cancellation of the output tone. We use an Agilent E4440A PSA Spectrum Analyzer for frequencies closer than 10 kHz

and an E5052A Signal Source Analyzer for frequencies farther than 10 KHz from the tone. The result is shown in Fig. 15. We show the close-in phase noise of several high-end commercial synthesized sources, the phase noise from the DAC including the clock source, and the phase noise contribution of the DAC itself. At 10 kHz offset of a 1 GHz carrier, the DAC noise is 21 dB lower than the best known commercial synthesizer.

To measure ACPR, a 4 channel WCDMA signal is received as complex baseband data at 300 MSa/s, interpolated to the DAC sample rate and modulated to an RF center frequency. The output directly from the DAC at 2.143 GHz achieves an ACPR of -73.7 dBc.

The built-in sweep capability can be used to generate reference-quality chirp signals with chirp rates as high as 5 GHz/ μ s. Fig. 16 shows amplitude vs. frequency, frequency vs. time and phase vs. time for a 500 MHz/ μ s chirp. The deviation from the theoretical parabolic phase trajectory is 0.8 degrees peak and 0.28 degrees RMS. A key figure of merit for chirp radar signals is the cross-correlation side lobe level, measured to be -52.7 dBc. This corresponds to approximately 0.3 degrees RMS of phase error[17].

A summary of measurement results for 14 bit and 12 bit modes is shown in Table 1.

Mode	14 bits	12 bits	Units
Specified Sample Rate	7.2	12	GSa/s
Max Sample Rate	9.9	13.6	GSa/s
Pout (with balun)	+1	+1	dBm

SFDR at $F_{OUT} < 100$ MHz	80	67	dB
SFDR, DC – Nyquist	67	55	dB
SNR for F_{OUT} at 1 GHz	66	61	dB
NSD	-161	-159	dBc/Hz

Table 1. Measured results summary.

Bipolar transistors require high current densities to reach high f_T and most bipolar circuits (both analog and digital) need supplies near three volts, so their power dissipation is high. The DAC portion of the chip and its high-speed clock buffers dissipate 8.3 W, including 1 W for the six stages of scaled ECL buffers in the clock circuit to stay within 30 fs RMS jitter budget. The high-speed MUX dissipates 5.0 to 8.3 W and the synthesized portion of the chip dissipates 3.1 to 6.5 W. Total power varies from 16.3 to 19.9 W. Performance was the primary design goal of the chip, with power consumption only of secondary importance to keep packaging cost contained.

VI. CONCLUSION

We have described a signal generator on a chip with integrated DAC that operates at 7.2 GSa/s with 14 bit resolution or at 12 GSa/s with 12 bit resolution. At 7.2 GSa/s it delivers at least 67 dB SFDR across the whole Nyquist region (80 dB SFDR for $F_{out} < 100$ MHz) and an SNR of 62 dB. It demonstrates -157 dBc/Hz phase noise at 10 kHz offset from a 1 GHz carrier, 22 dB better than known synthesized signal generation instruments. Digital INL suppression, a DSP-clock-to-analog-output isolation of 128 dB and distributed resampling applied to all current sources in the DAC contributed to the dynamic performance. Digital sub-harmonic suppression

and logic activity randomization were designed into the chip but not necessary to achieve the dynamic performance thanks to (a.o.) the excellent isolation. The chip features interpolation of IQ data (up to 480 MHz), an agile DDS engine (CW, chirp sweep) and AM, FM and PM modulation. The digital signal generation, interpolation and modulation capabilities, combined with impairment corrections for the high-speed, high resolution DAC allow a simplification of block diagrams across a wide range of instrumentation-quality applications.

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LIST OF FIGURES

Fig 1. Chip block diagram.

Fig. 2. Simplified DAC block diagram showing Sub-DACs A & B. Data to Sub-DAC B is delayed one half clock cycle.

Fig. 3. Simplified schematic of a DAC current source and switching

Fig. 4. Digital signal processing.

Fig. 5. Activity Scrambling in an Interpolator Stage.

Fig. 6. Numerically Controlled Oscillator.

Fig. 7. Upper: Phase-continuous switching – no jump in phase or voltage
 Lower: Phase-repeatable switching – jumps to the original phase trajectory

Fig. 8. Current Source Error Correction.

Fig. 9. Chip die photo.

Fig. 10. INL, Showing effects of DEM and CSEC.

Fig. 11. Output spectrum. $F_{OUT} \approx 2.2$ GHz tone, $F_S = 7.2$ GSa/s.

Fig. 12. SFDR vs. F_{OUT} at $F_S = 7.2$ GSa/s and $F_S = 12$ GSa/s.

Fig. 13. SFDR vs. F_S .

Fig. 14. DC-Nyquist SFDR at various sample rates vs. other DACs.

Fig. 15. Close-in phase noise at 1 GHz F_{OUT}

Fig. 16. 500 MHz/ μ s frequency sweep centered at 1 GHz with 500 MHz span.

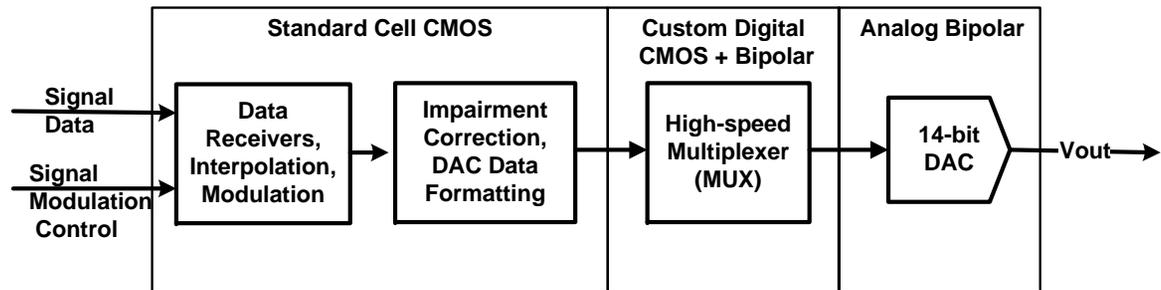


Fig 1. Chip block diagram.

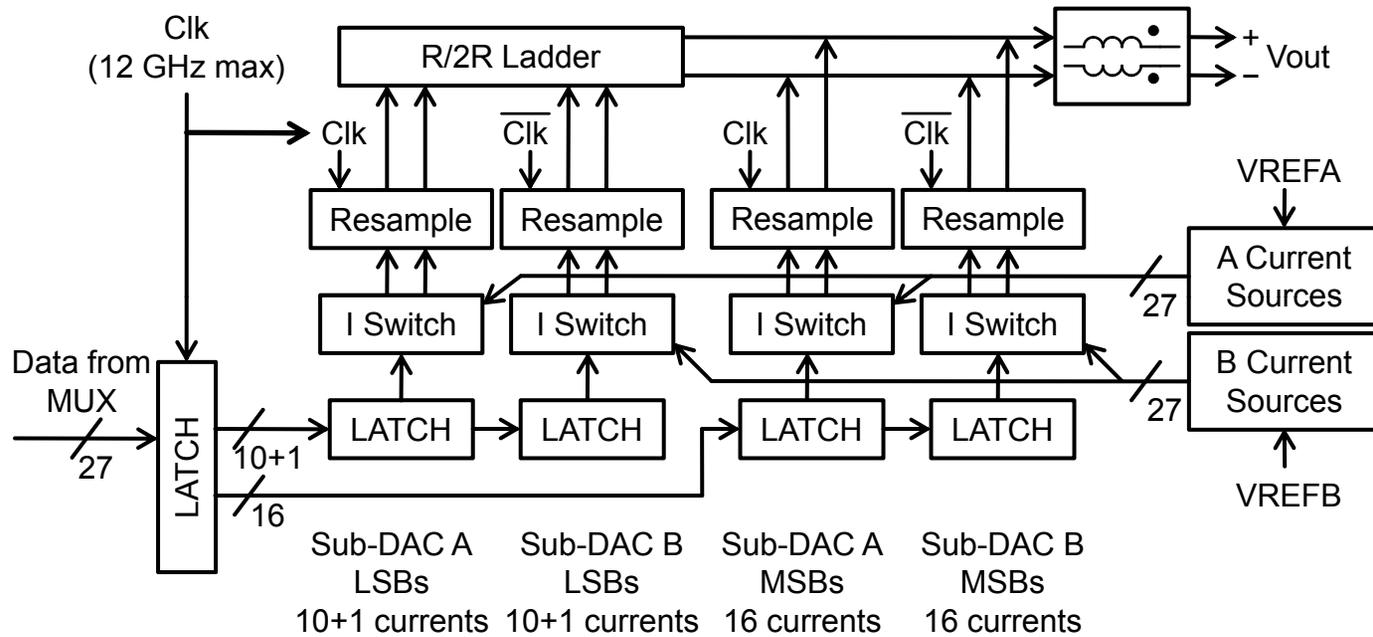


Fig. 2. Simplified DAC block diagram showing SubDACs A & B. Data to SubDAC B is delayed one half clock cycle.

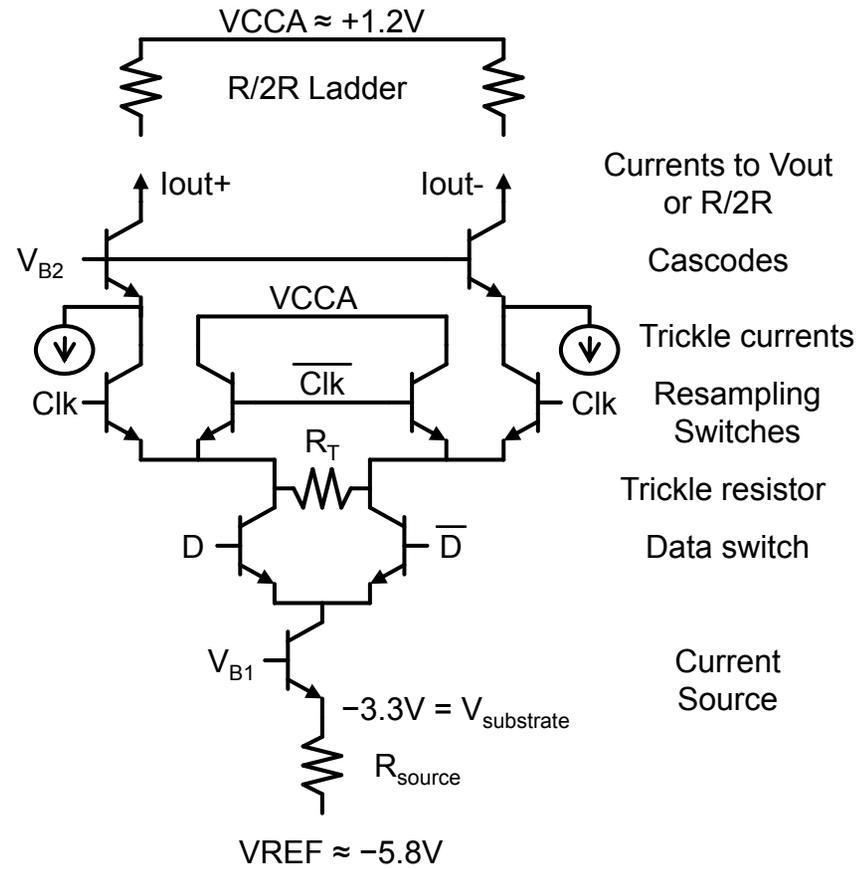


Fig. 3. Simplified schematic of a DAC current source and switching

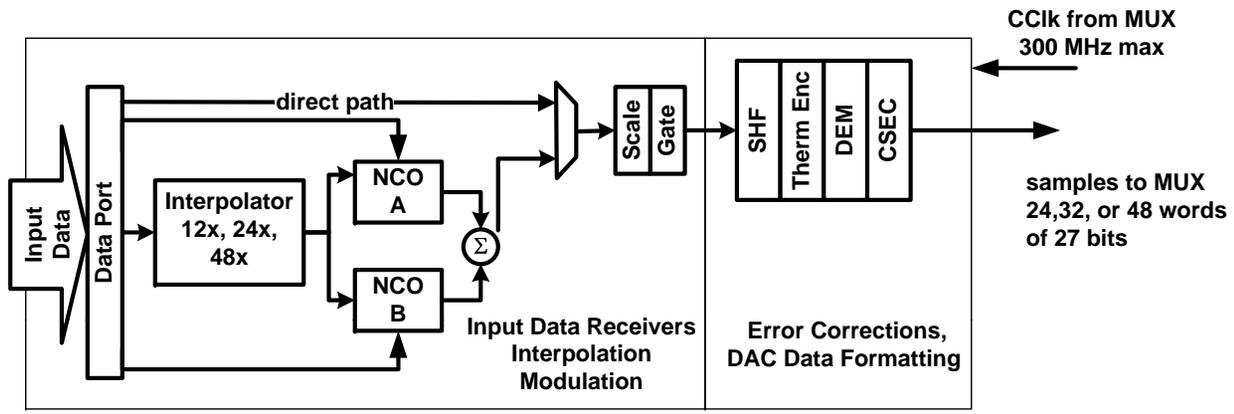


Fig. 4. Digital signal processing.

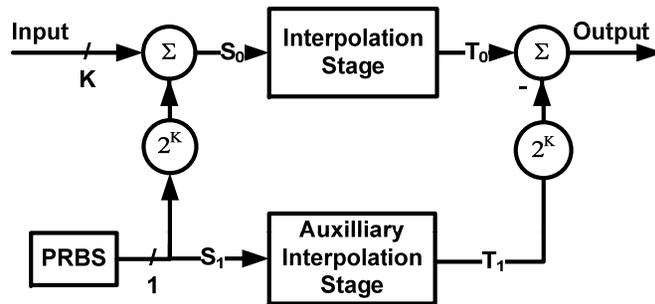


Fig. 5. Activity Scrambling in an Interpolator Stage.

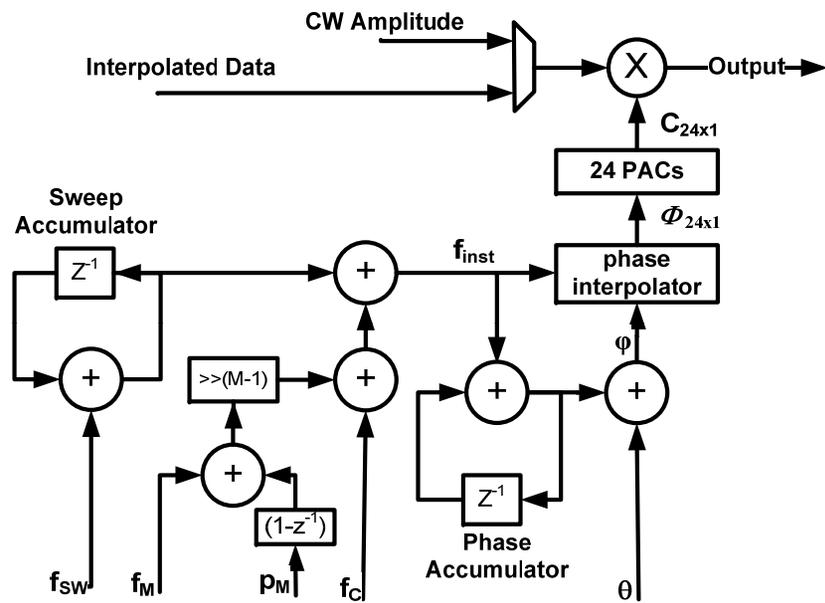


Fig. 6. Numerically Controlled Oscillator.

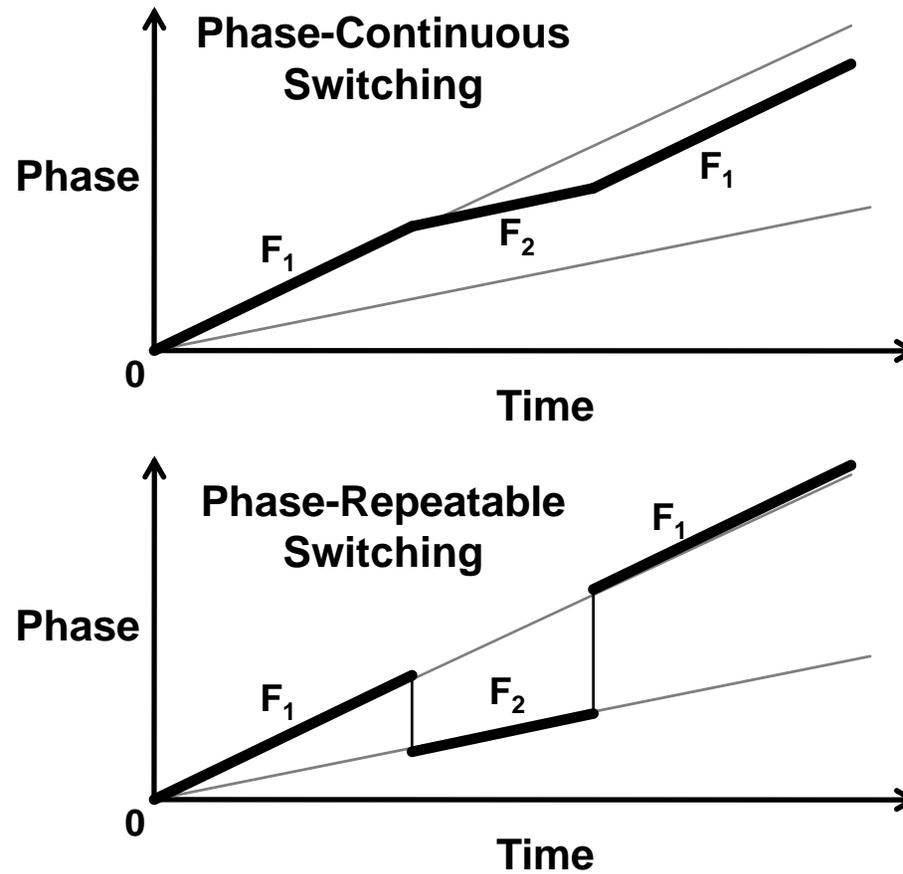


Fig. 7. Upper: Phase-continuous switching – no jump in phase or voltage
Lower: Phase-repeatable switching – jumps to the original phase trajectory

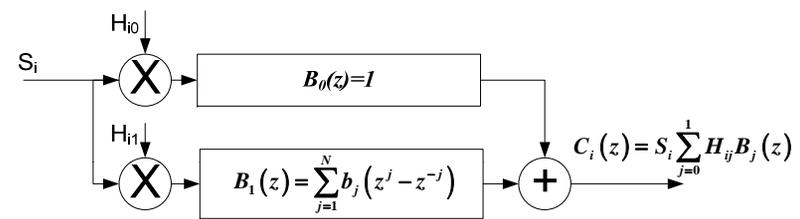


Fig. 8. Current Source Error Correction

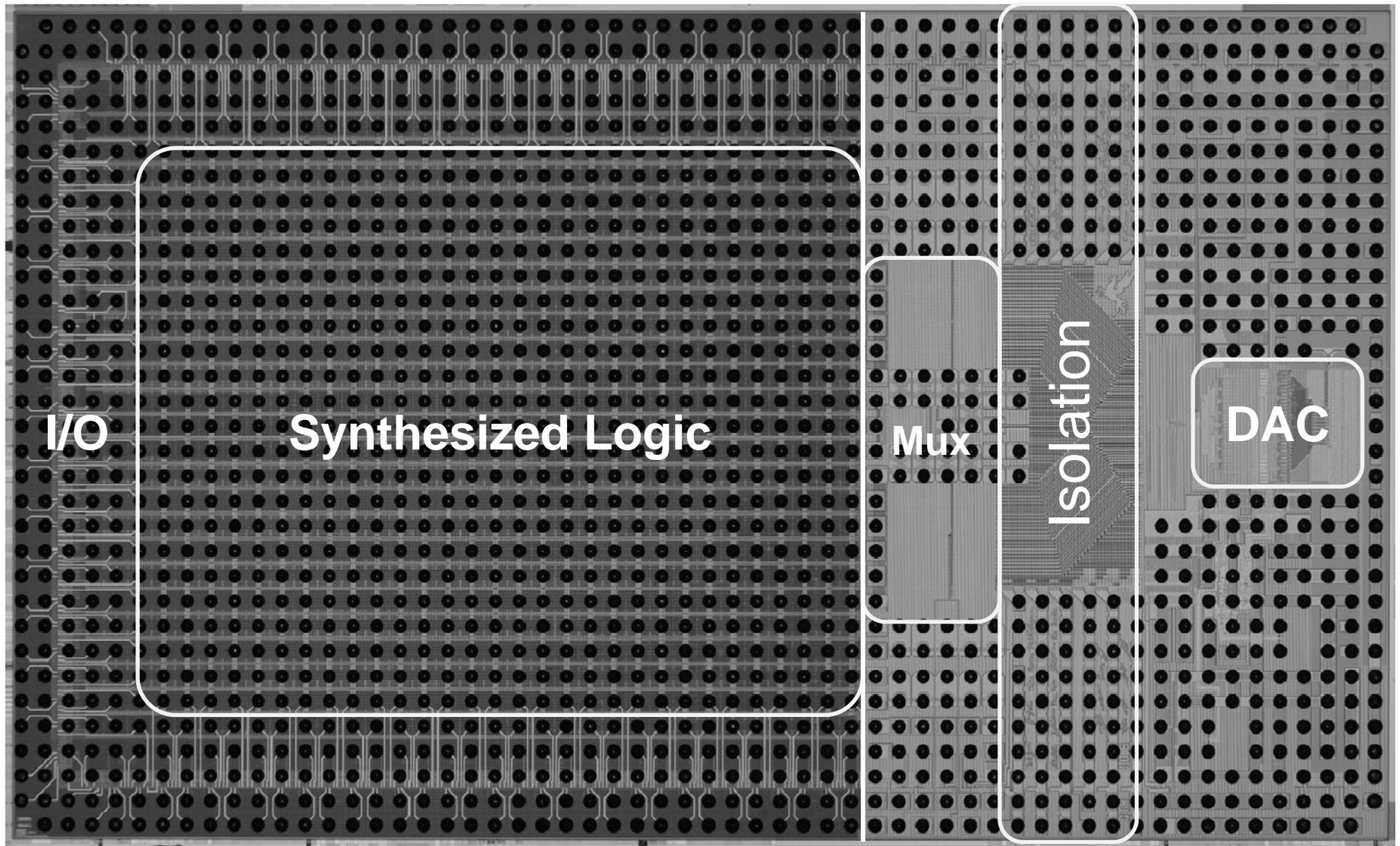


Fig. 9. Chip die photo.

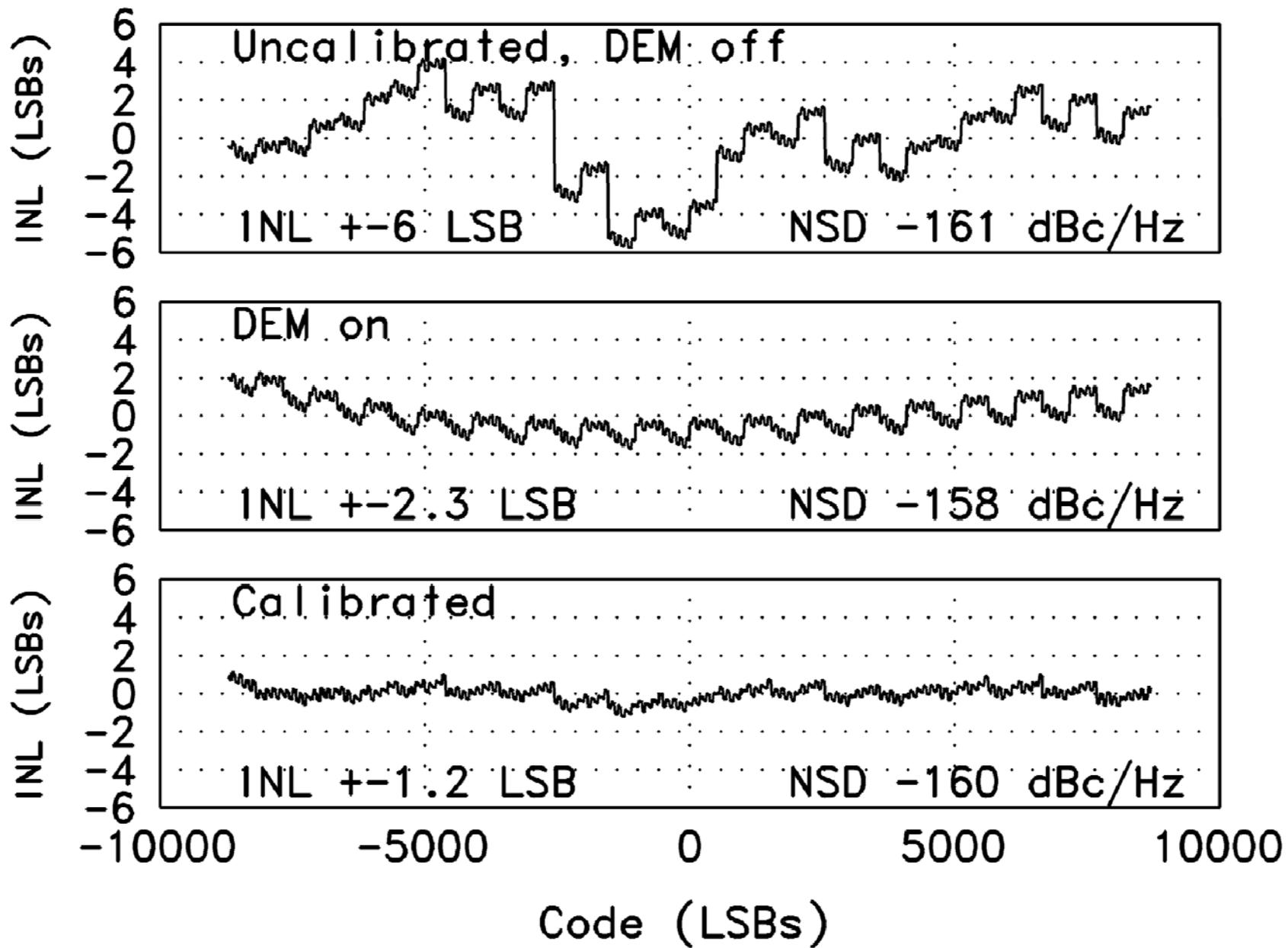


Fig. 10. INL, Showing effects of DEM and CSEC.

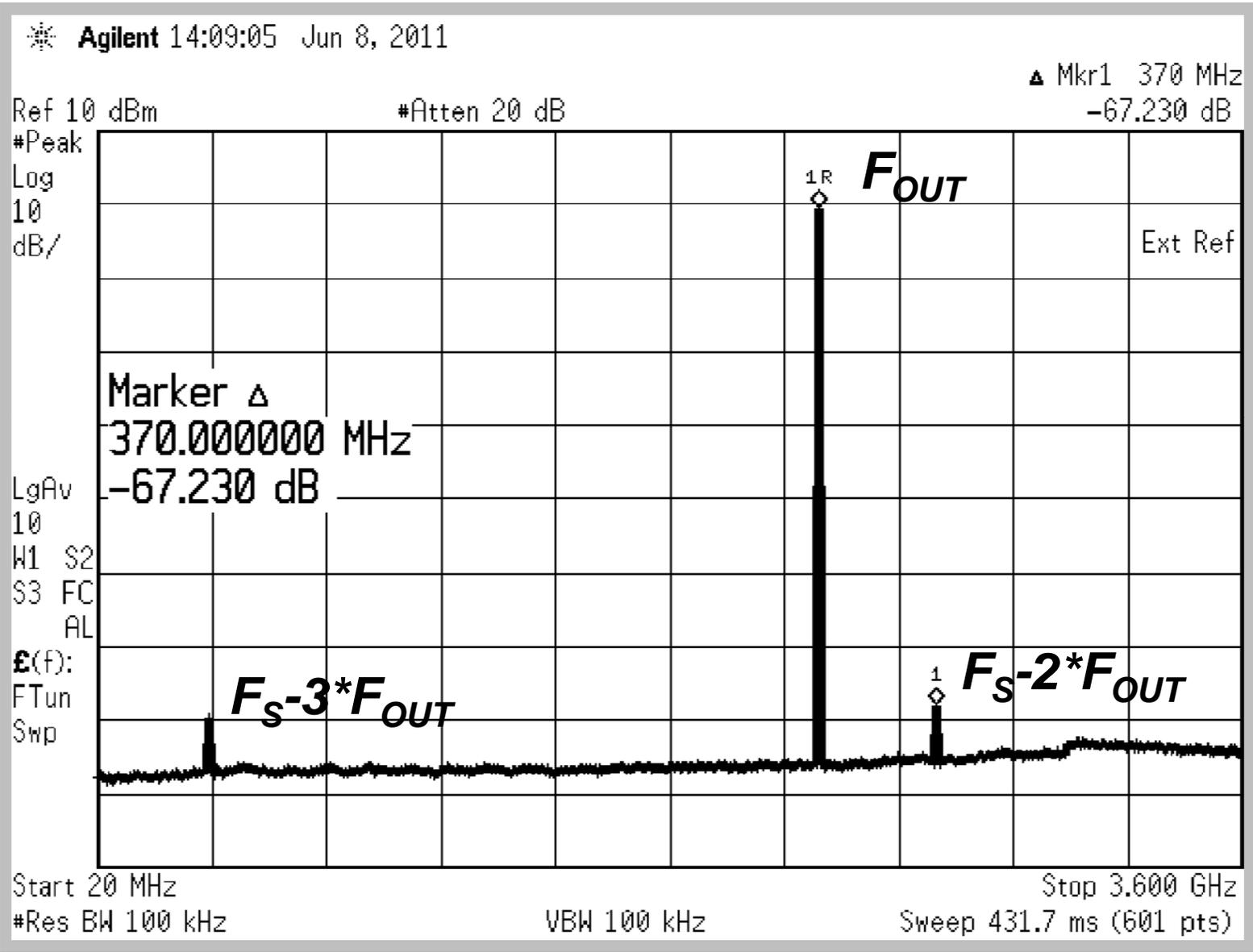


Fig. 11. Output spectrum. $F_{OUT} \approx 2.2$ GHz tone, $F_S = 7.2$ GSa/s.

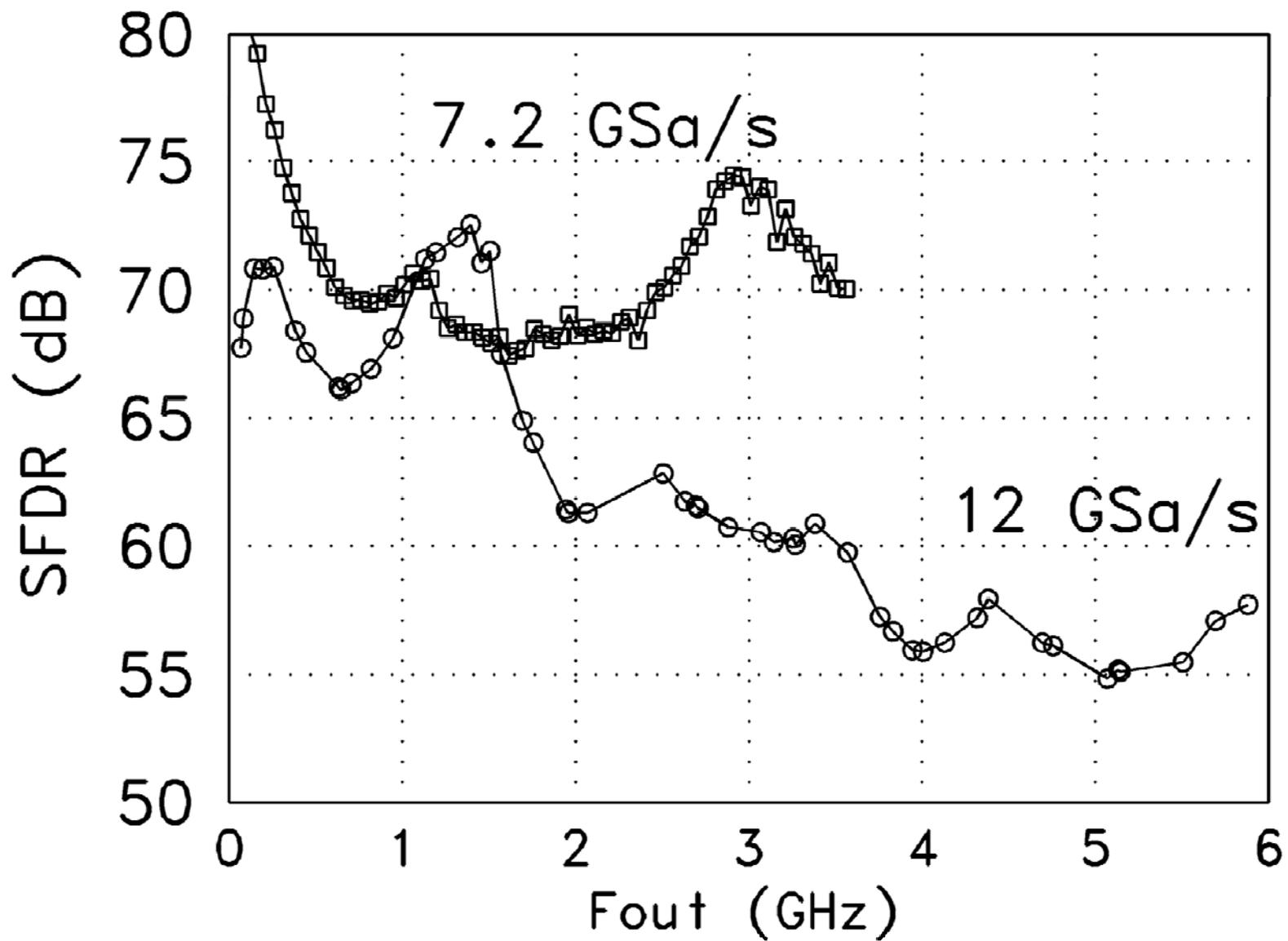


Fig. 12. SFDR vs. F_{OUT} at $F_S=7.2$ GSa/s and $F_S=12$ GSa/s.

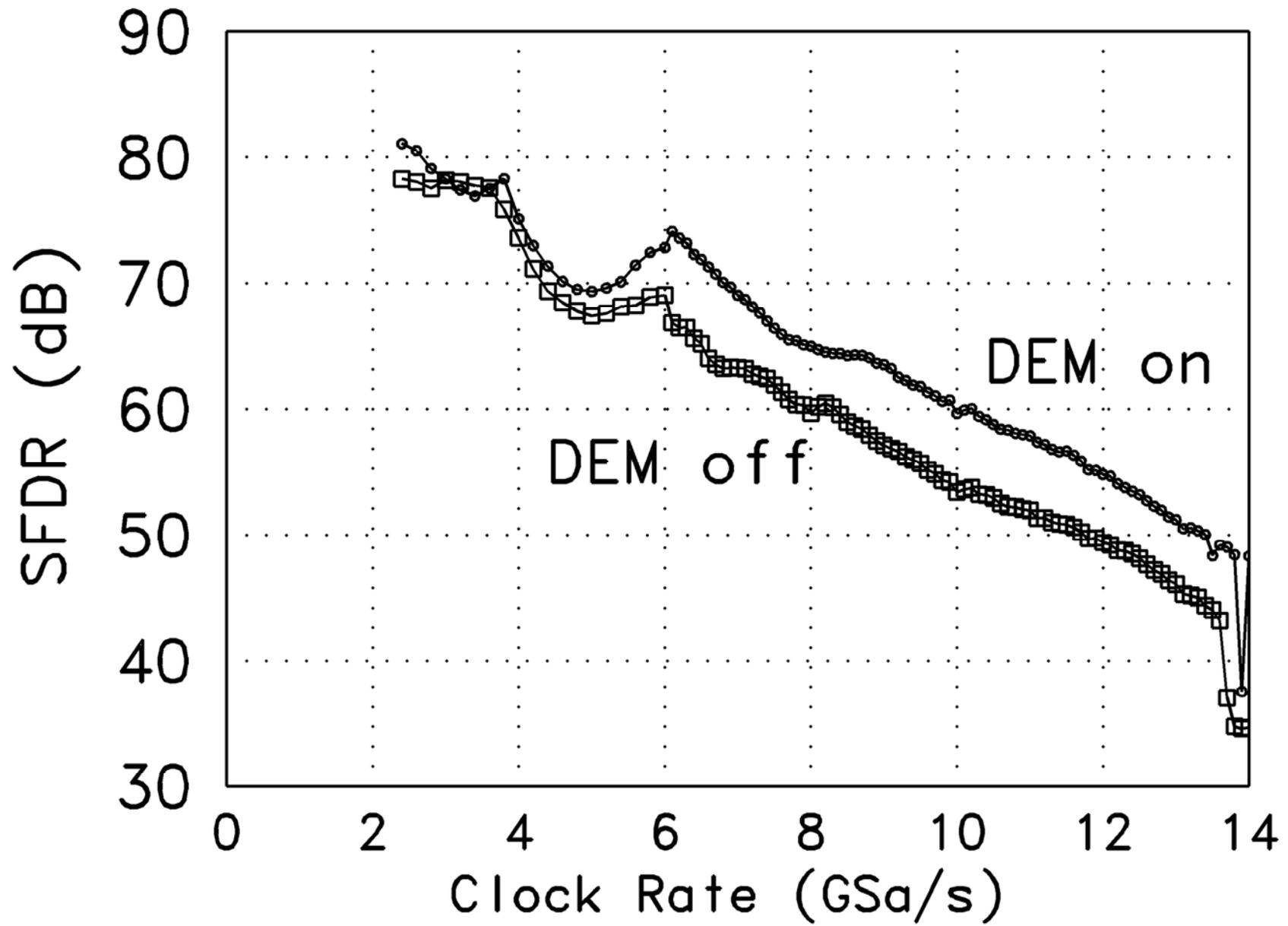


Fig. 13. SFDR vs. F_S .

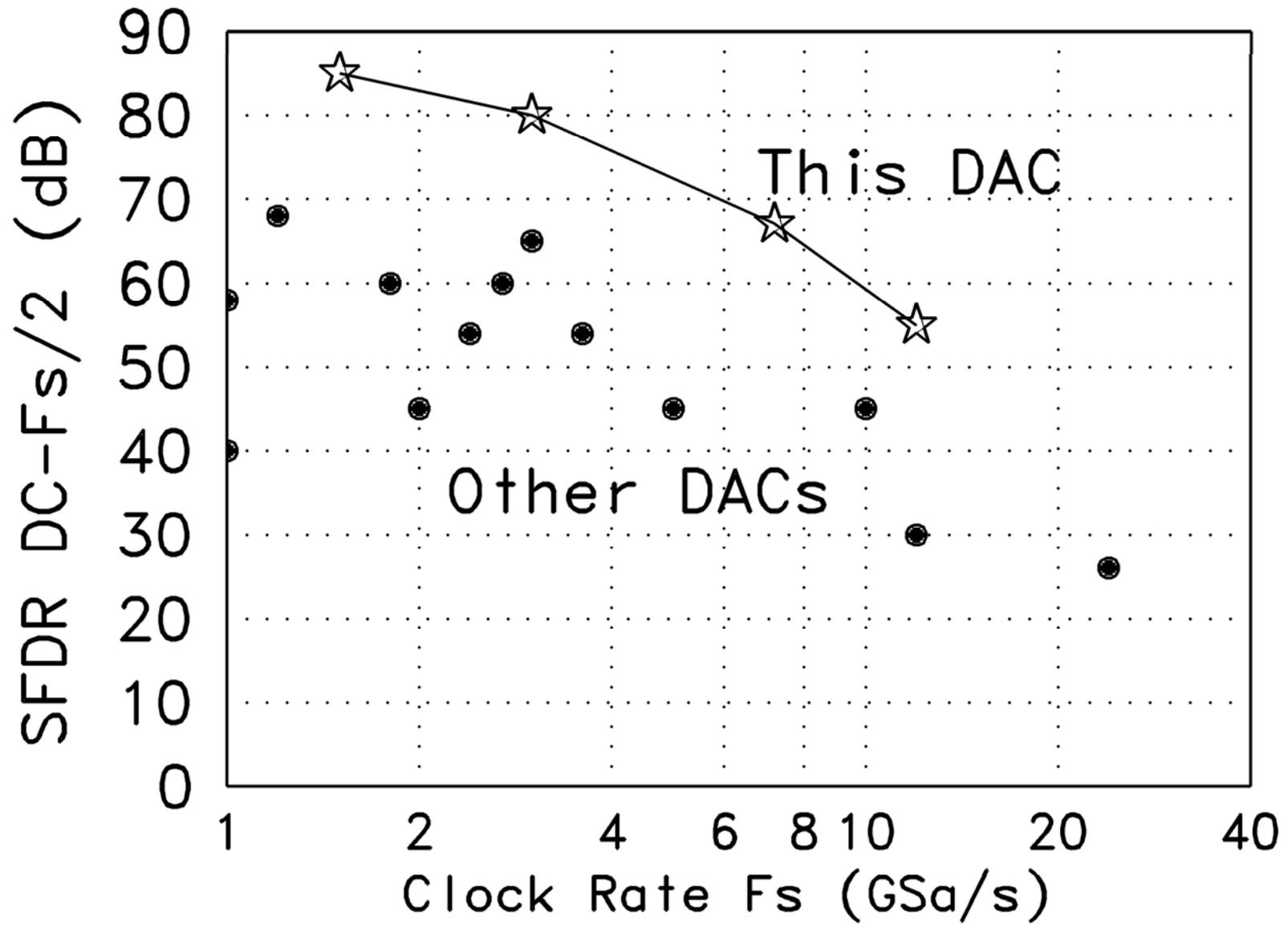


Fig. 14. DC-Nyquist SFDR at various sample rates vs. other DACs.

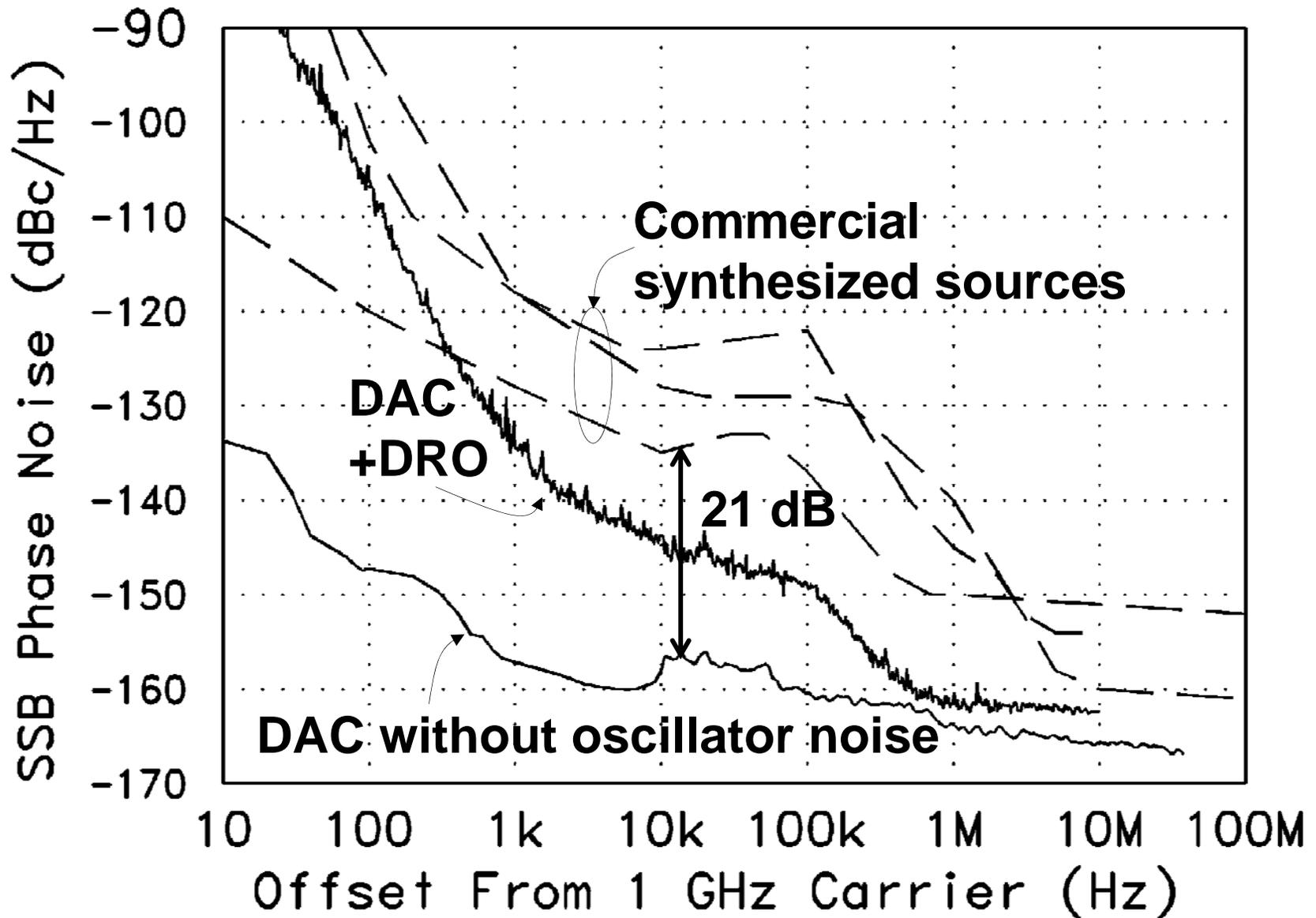


Fig. 15. Close-in phase noise at 1 GHz F_{OUT} .

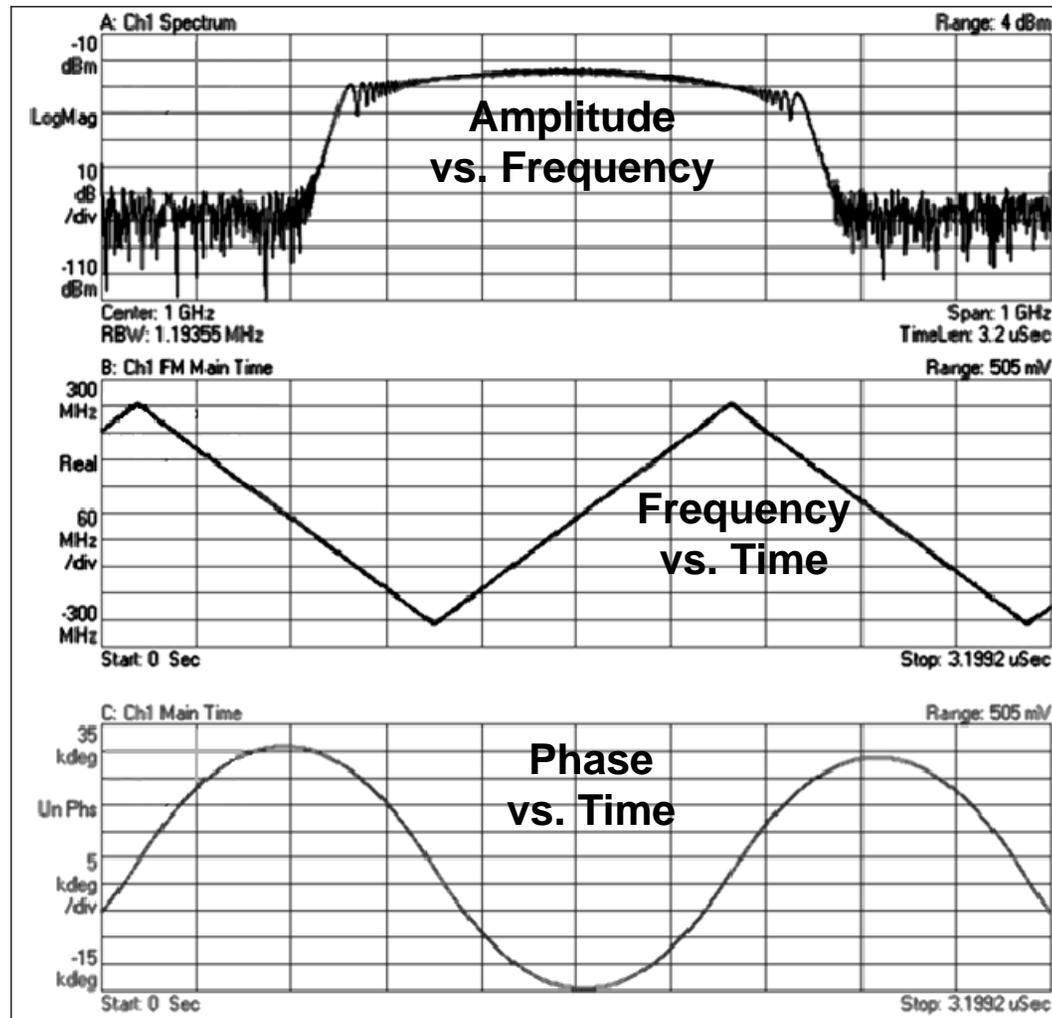


Fig. 16. 500 MHz/ μ s frequency sweep centered at 1 GHz with 500 MHz span.