A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz f_T BiCMOS Process

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Abstract

We describe a DAC which can operate at up to 7.2 GSa/s with 14-bit resolution or up to 12 GSa/s with 12-bit resolution. It uses a segmented architecture, with an R/2R ladder for the 10 LSBs; distributed resampling is applied to all current sources. The DAC achieves an SFDR of 77 dB at low output frequencies and an SFDR of 67 dB and an SNR of 62 dB from DC to 3 GHz. It demonstrates a phase noise of -157 dBc/Hz at 10 kHz from a 1 GHz carrier, 22 dB better than synthesized signal generation instruments.

The DAC is built in a 165-GHz f_T, 130-nm BiCMOS process and packaged in a 780-ball BGA.

Keywords: DAC, BiCMOS, 14-bit, resampling, SFDR, phase noise, R/2R

Introduction

High-speed, high-resolution digital-to-analog converters (DACs) are central to RF signal generation for wireless networking, cellular communications, radar and instrumentation applications. Increasing the sample rate and bandwidth of the DAC allows a system to be built with fewer RF mixing, filtering and switching components after the DAC. If the DAC is fast enough, no further frequency translation is needed, which can enable simpler systems with performance limited only by the DAC.

Design

This DAC chip operates at up to 7.2 GSa/s with 14-bit resolution. It can also operate at up to 12 GSa/s with the input pins reconfigured for 12-bit data to keep the data interface at no more than 1 Gb/s/pair. To our knowledge, these are the fastest DAC sample rates at these resolutions.

The core of the chip is a 14-bit segmented DAC with 16 unary current sources representing the 4 MSBs. Ten equal-size current sources are given binary weighting by an R/2R ladder to represent the 10 LSBs. Distributed resampling[1] on each DAC current enables the DAC to achieve high SFDR over the whole Nyquist band.

The chip is fabricated in a BiCMOS process with 165-GHz f_T NPNs and 130-nm CMOS. The DAC core and its data multiplexor circuits are mostly built using bipolar devices; the data inputs, control and digital coding and correction circuits are synthesized in standard-cell CMOS.

A. Analog Circuits

Figure 1 shows the DAC simplified schematic. Resampling a DAC output can improve performance by suppressing the nonlinear glitches that occur at DAC transition times. A single resampling switch on the output of a DAC tends to suffer from switching glitches which vary with the current in the output signal.

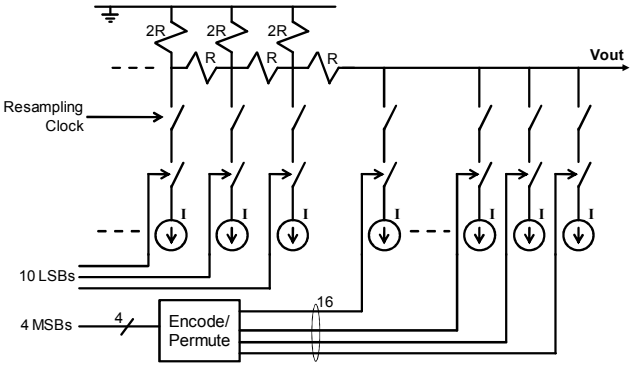

Fig. 1 DAC Core simplified schematic

Distributed resampling uses one switch per current source, all driven with a common clock. The resampling occurs before currents are sent into the R/2R ladder, so that each of the resampling switches (LSBs as well as MSBs) operates on the same unit current (2 mA) so that a) the switch timing is independent of the total DAC output current and b) the switches all operate simultaneously.

Figure 2 shows the schematic of the differential current

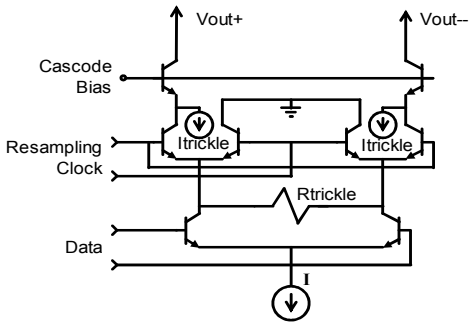

Fig. 2 DAC current switch

switching cell. The cell includes a per-current cascode to isolate the resampling devices from the analog output swing and reduce wiring capacitance at the output node. It also uses a resistor $R_{trickle}$ to keep a small current flowing in the resampling devices and currents $I_{trickle}$ to keep a small current in the cascodes. This avoids long time constants at these devices' emitters which can cause "memory" effects.

The resampling creates an RZ output waveform with 6 dB lower output power, so two DAC cores are used, clocked half a clock cycle apart. This recreates an NRZ waveform. Note that these two cores use the same data, so, unlike many DACs over 1 GSa/s, this DAC acts as a single NRZ DAC clocked at the full sample rate and there are no interleaving spurs.

Clocking is key to the distributed resampling architecture. The clocks in the DAC core are distributed in binary trees to the resampling switches; a second clock tree drives the data latches driving the current switches for uniform alignment with the resampling clock.

B. Digital Circuits

The digital data path includes 144 LVDS data pairs with 4 clock pairs which receive input parallel data words at up to 1 Gb/s per pair.

To reduce the effects of MSB current mismatch, the digital section includes thermometer coding and pseudo-random permuting of the MSBs as well as digital correction of current source errors. It also includes 5 million gates of other synthesized logic which is outside the scope of this paper.

C. Analog/Digital Isolation

An advantage of using a BiCMOS process is the opportunity to put complex digital circuits in CMOS on the same chip as the bipolar DAC. However, the CMOS logic must run at much lower clock rates (e.g., 250 MHz) which brings the risk of the CMOS clock leaking directly into the analog output or mixing with the analog output. This chip includes many measures to suppress this leakage, including: separate analog and digital supplies including ground, keeping supplies separate in the package as well, use of a process with a resistive (low-doped) substrate, and a 1.5-mm physical isolation region between the analog and digital sides of the chip (Fig. 4).

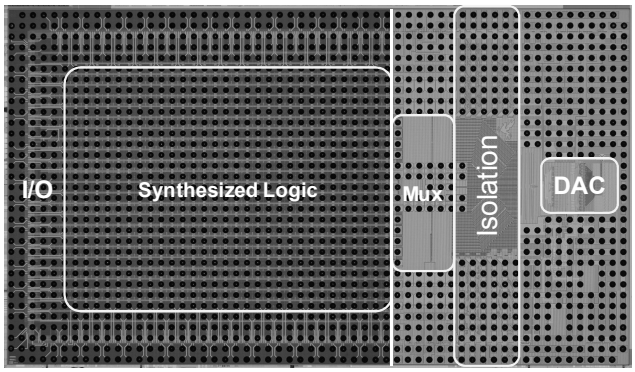

Fig. 4 Chip Photo

The chip is 14 x 8 mm. It is flip-chip attached to a custom multi-layer ceramic BGA with 780 balls.

Measured Performance

The DAC is tested on a custom PC board using a balun on the outputs to suppress even harmonic distortion.

SFDR and SNR are shown in Fig. 5. At 7.2 GSa/s, the DAC achieves over 77 dB SFDR at low output frequencies and 67 dB SFDR from DC to 3.6 GHz. The SNR (with current source calibration turned on) is 72 dB at low output frequencies and 63 dB at 3 GHz. The broadband noise spectral density is better than -160 dBc/Hz; it is dominated by the 30 fs rms jitter of the clock input buffer chain.

At 12 GSa/s, the SFDR is 55 dB from DC to 5 GHz and SNR is better than 62 dB. Fig 6 shows that this DAC's SFDR across the Nyquist region is 10 dB better than other known DACs at similar sample rates.

Fig 7 shows the phase noise of the DAC (not including the clock source). At 10 kHz from a 1 GHz carrier, it is 22 dB better than the best known synthesized signal generation instruments.

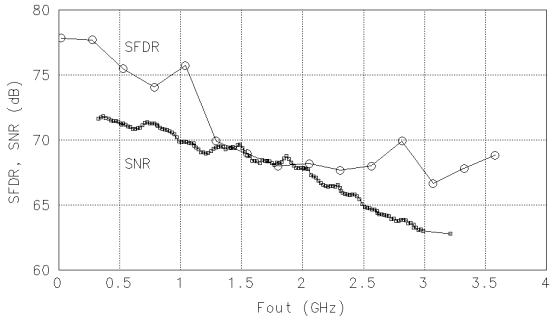

Fig. 5 SFDR (including harmonics) and SNR vs. Fout at 7.2 GSa/s

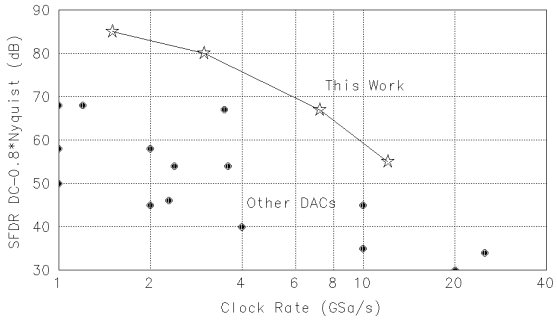

Fig. 6 SFDR over Nyquist vs clock rate for this DAC and other DACs (published papers and datasheets)

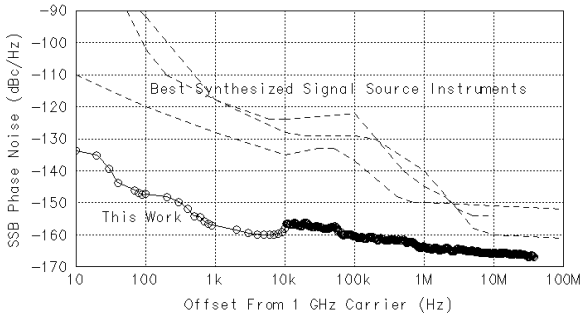

Fig. 7 Phase noise at 1 GHz of this DAC at 7.2 GSa/s and of synthesized signal generator instruments

The analog/digital isolation was tested with 3 W of dissipation in the CMOS logic; feedthrough spurs and mixing spurs due to the CMOS clock are below -90 dBm, giving an on-chip power-ratio isolation of 125 dB.

Signal output power is 0 dBm at 3 GHz Fout. INL is ±10 LSBs without correction, and ±0.8 LSB with correction. The DAC power is 4.6 W, not counting the digital I/O and multiplexing.

Acknowledgements

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References

[1] Bob Jewett, Jacky Liu, Ken Poulton, "A 1.2 GS/s 15b DAC for Precision Signal Generation", *IEEE International Solid State Circuits Conference Digest of Technical Papers*, pp 110-111, Feb 2005