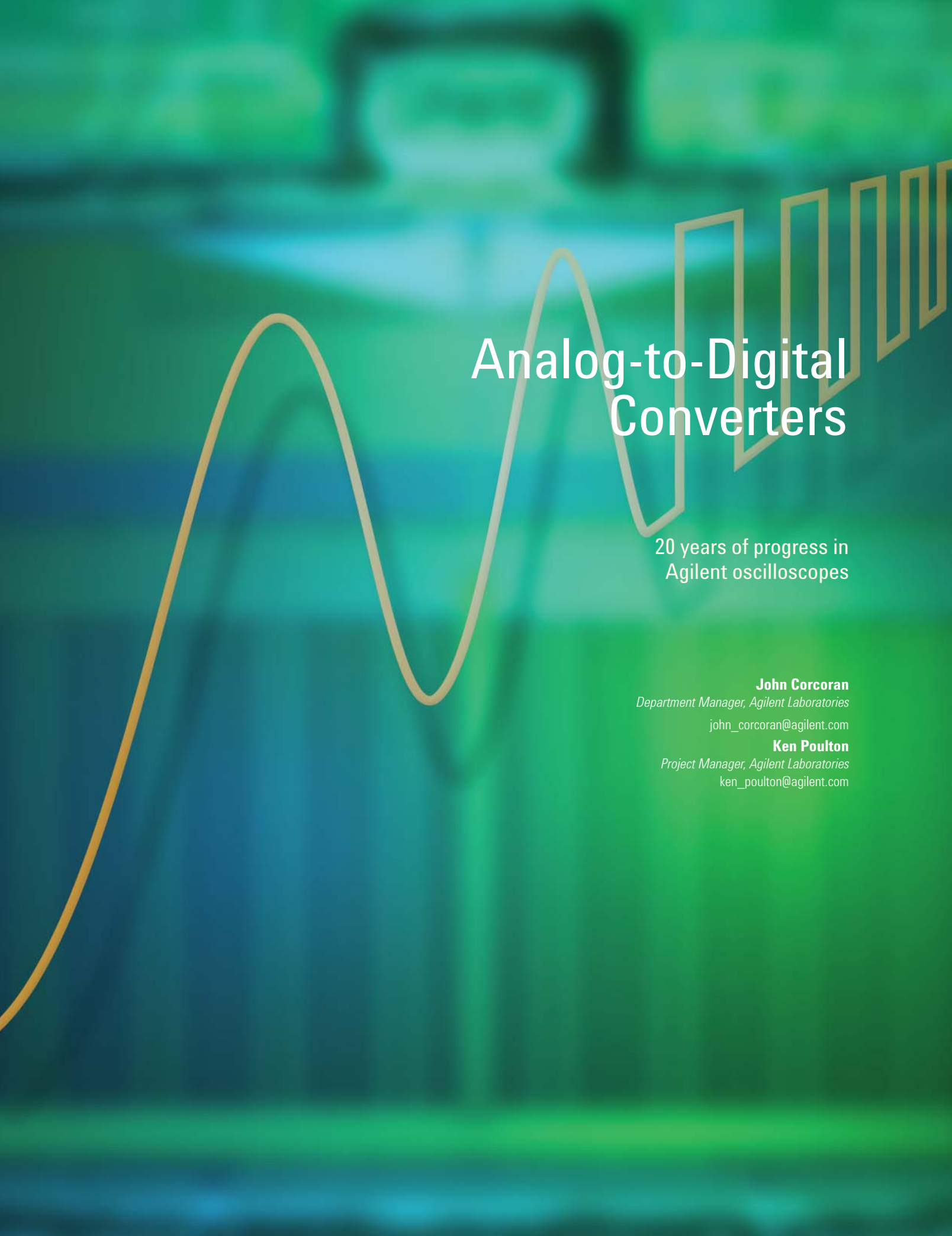

# Analog-to-Digital Converters

## 20 years of progress in Agilent oscilloscopes

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Over the past 20 years, the real-time (transient capture) bandwidth of Agilent Technologies' oscilloscopes has increased by more than 40 times, from 250 MHz in 1987 to 13 GHz today. An enabling factor in achieving this increase in bandwidth is the sample rate of the internal analog-to-digital converter (ADC) which digitizes the oscilloscope input signal for storage in digital memory.

Correspondingly, Agilent's scope ADC sample rates have grown from one gigasample/second (1 GS/s) in 1987 to 40 GS/s today. In this article we will review how scope ADC architectures have been optimized over the past two decades to best exploit the available integrated circuit (IC) technology and enable this performance increase. To do this, we will describe three benchmark ADC designs, one from 1987, one from 1997, and the ADC in use in Agilent's high-end oscilloscopes today.

How does a 40:1 increase in ADC sample rate correspond to the progress due to Moore's Law over the past two decades? Moore's Law, of course, describes the amazing increases in MOS integrated circuit density and performance due to scaling — the result of shrinking transistor sizes. We can perhaps use personal computer (PC) clock rate as a measure of the progress due to Moore's Law. If you bought a new PC in 1987, you were performing your word processing on a microprocessor with about a 25 MHz clock rate. In 1997, you could buy a PC with close to 250 MHz clock rate. Today, PCs are available with clock rates of 2.5 GHz or higher. So, roughly speaking, progress under Moore's Law has delivered a factor of 100 in PC clock rate over the past 20 years.

However, this progress in MOS IC technology is not solely responsible for the progress in ADC sample rates. In 1987, it was not possible to build a 1 GS/s ADC with MOS IC technology. The fastest IC technologies available at that time were based on GaAs FET and silicon bipolar transistors. Although neither of these were a good choice for building a microprocessor, they were the right choice if you wanted to build the world's fastest scope ADC. In 1997, silicon bipolar technology had evolved to higher speeds and obviated the need for GaAs FETs, allowing a more compact design. By the turn of the century, however, CMOS technology had caught up with bipolar technology in throughput, if not in raw speed, and offered intriguing possibilities for very high speed ADCs. But as we will describe later, exploiting CMOS for ADCs required substantial ADC architecture and system design changes.

## Types of oscilloscopes

There are two types of oscilloscopes in common use today, usually called sampling oscilloscopes and real-time oscilloscopes. To understand the motivation for building very high sample rate ADCs for scopes, it is important to understand the difference.

### Sampling oscilloscopes

Sampling scopes are typically very high bandwidth (up to 80 GHz today). But to get that high bandwidth, they use samplers that operate at low sample rates, typically under 1 MHz. Sampling scopes work only with repetitive signals, and those signals are typically sequentially digitized. First, a clock synchronized with the input signal triggers the oscilloscope to capture a sample. After that sample is digitized the trigger input is re-armed. When the next clock occurs, a small delay is introduced before taking another sample. With each successive clock signal, larger delays are introduced. In that way, the signal is sequentially "traced out" by the scope (see the sine wave example of Figure 1).

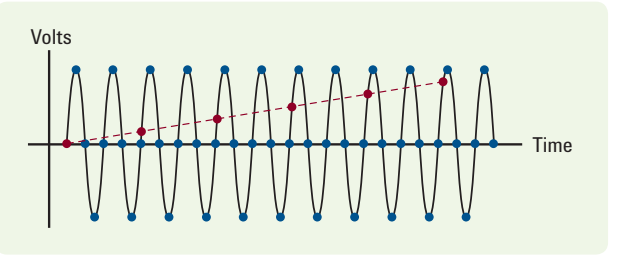


**Figure 1. Sampling scopes (red dots) acquire a single cycle of the signal only after multiple repetitions. Real-time scopes (blue dots) acquire the same signal in a single occurrence.**

Sampling scopes are often used for characterizing the quality of high-speed communication signals by displaying eye diagrams. In these signals bandwidth is often very high and the signal is repetitive, so sampling scopes are a very good match.

**Real-time oscilloscopes**

Real-time scopes capture a complete image of the input signal in a single occurrence — they can even capture one-time events. To do this, the sample rate of the ADC must be more than twice the bandwidth of the signal being captured. Most scopes use ratios between 2.5 and 4 to allow for implementation of practical reconstruction filters for best waveform fidelity.

Real-time scopes are most commonly used in debugging digital systems, where infrequent glitches can occur — sometimes crashing the system. These glitches would be missed by a sampling scope, but are completely captured by a real-time scope if it has adequate bandwidth. Likewise, serial communication signals in use in PCs today (such as Serial ATA and PCI Express) may occasionally have bit errors. A real-time scope can capture the complete signature of such an error and accelerate system debugging. Digital systems today have multi-GHz clock rates, and modern serial communication systems operate at 2.5 Gb/s, 5 Gb/s, or even 10 Gb/s. These applications demand very high bandwidth real-time scopes, and therefore, very high sample rate ADCs.

## Real-time scopes — historical overview

Since 1980, Agilent Technologies, Inc.* has introduced digitizing oscilloscopes using nine custom-designed analog-to-digital converters ICs. A number of these converters were designed at Agilent Labs, others at Agilent business units[1]. For the purpose of this article we will focus on the design choices of just three ADCs (from 1987, 1997, and today) that highlight the evolution of IC technology and ADC architectural changes over the past 20 years.

In 1987, Agilent introduced the world's first oscilloscope with a 1-GS/s ADC, the 54111D (see Figure 2). The key enabling technology was a GaAs FET sampler chip that drove four silicon bipolar digitizers. Ten years later, in 1997, silicon bipolar technology had increased in $f_T$ (transistor cutoff frequency) by a factor of five. Along with architectural changes, this enabled an 8-GS/s ADC system using only bipolar technology. A family of scopes was introduced that used this ADC, including the Agilent 54845A (as shown in Figure 3) which had 1.5 GHz bandwidth. Most recently, 0.18-micron CMOS technology was exploited to enable a 40-GS/s scope channel. Memory was built into the ADC chip for capturing the digitized data. Agilent's fastest real-time scope is the DSO81304B (as shown in Figure 4) which samples at 40 GS/s with 13 GHz bandwidth.

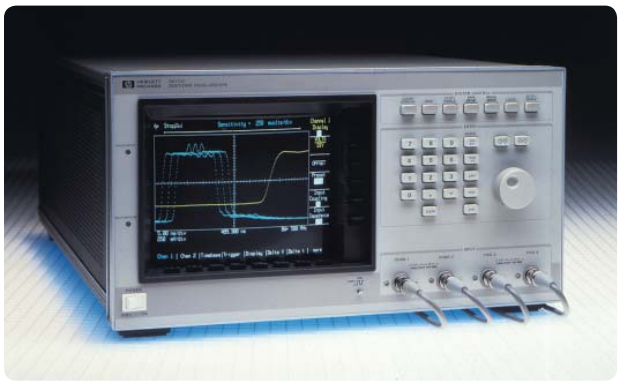

**Figure 2. 54111D 1-GS/s digitizing oscilloscope**

**Figure 3. 54845A**

Heidi,

We use the following in Roger Stancliff's Evolution of Network Analyzers article:

*All products mentioned in this article prior to 2000 were sold under the Hewlett-Packard name. This was the year that Agilent Technologies, Inc. was spun out of Hewlett-Packard as an independent company.

Should they match and if so which should we edit?

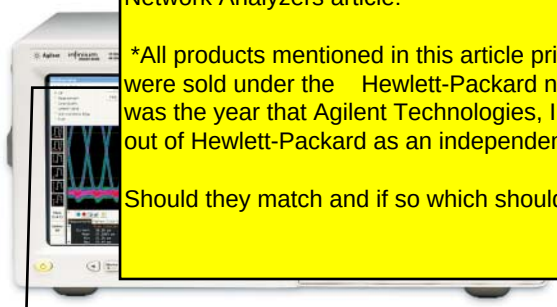

**Figure 4. DSO81304B 40 GS/s Infiniium oscilloscope**

*All technologies and products mentioned in this article prior to 2000 were developed and sold under the Hewlett-Packard name.

It is interesting to compare the performance of these ADCs and scope channels across various measures (see Table 1). From 1987 to today, sample rate increased by 40 times, bandwidth by 52 times, resolution by 2 bits (or 4 times), and memory depth by 250 times. Power, interestingly, stayed about the same at 20 W per ADC channel, with memory included. But power efficiency, measured in watts per gigasample, dropped from 20 to 0.5, for a 40 times improvement. Given the nominal 2 extra bits of resolution, the figure of merit of power/gigasample per conversion step has improved by 160 times.

**Table 1. Progress in ADC performance since 1987.**

| | 1987 | 1997 | Today | Today vs 1987 |
|---|---|---|---|---|
| Sample rate | 1 GS/s | 8 GS/s | 40 GS/s | 40x |
| Real-time bandwidth | 250 MHz | 1.5 GHz | 13 GHz | 52x |
| Resolution | 6 bits | 8 bits | 8 bits | 4x |
| Memory depth | 8 kB | 64 kB | 2 MB | 250x |
| Power | 20 W | 27 W | 20 W | 1x |
| Watts/gigasample/s | 20 | 3.4 | 0.5 | 40x |
| Chip count | 10 | 4 | 2 | 5x |

## 1987: The world's first 1-GS/s 6-bit ADC

Bipolar IC technology was the logical choice for ADCs in the 1980s due to its excellent device matching and relatively high device speeds (5 GHz $f_T$). This technology was capable of building a 400-MS/s 6-bit ADC on one chip using a modification of the flash ADC architecture, with about 100 MHz of input bandwidth[2]. However it was clear that the marketplace required sample rates of 1 GS/s, and analog bandwidths as high as 1 GHz for use with repetitive signals.

The solution for the sample rate shortfall was to time-interleave multiple ADC ICs. Four such chips, each operating at 250 MS/s (a 4 ns period), but clocked sequentially 1 ns apart, would supply an aggregate sample rate of 1 GS/s. To improve the bandwidth, a sample and hold circuit would precede each digitizer (ADC) as shown in Figure 5. GaAs FET technology was chosen for this role, due to its 14-GHz transistor $f_T$ and high-speed Schottky diodes, which are well suited to sample and hold applications. All four samplers would be integrated on one GaAs chip.

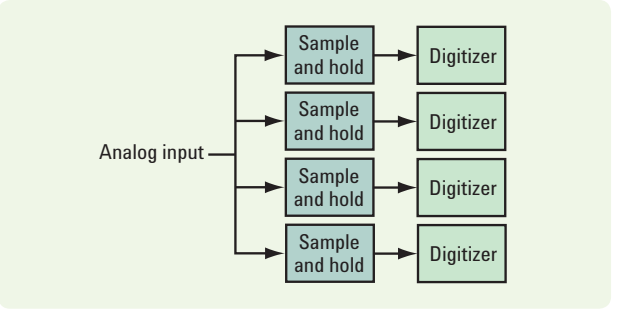


**Figure 5. Four 250 MS/s sample and hold circuits and ADCs are time-interleaved to produce a 1 GS/s system.**

However, a significant problem remained. When using time-interleaved samplers to capture a fast input signal, errors are introduced if the sampler clocks are not precisely timed (see Figure 6). To achieve 6-bit accuracy at a 1 GHz input frequency, the clocks would have to be timed to an accuracy of 2 ps, and this was judged to be impractical. The solution was to add a 1-GS/s first rank sample and hold circuit to the GaAs chip (see Figure 7). This sampler distributed settled samples to the four second rank samplers in turn. Because the second rank inputs were not moving when sampled, precise timing of their clocks was no longer required.

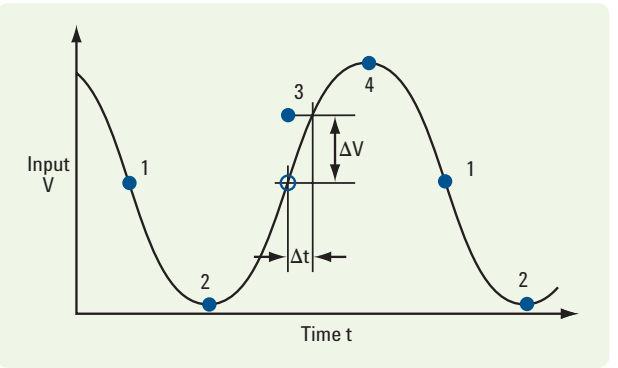


**Figure 6. A small sample and hold timing error can produce a significant error in the sampled voltage.**

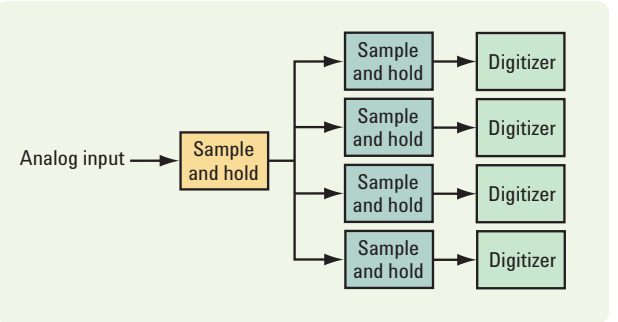


**Figure 7. A two-rank sample and hold system, with the first sampler operating at 1 GS/s, can eliminate sensitivity to interleave timing errors.**

A complete block diagram for the 1-GS/s ADC system is shown in Figure 8. A second GaAs chip was used to supply the clocks for the system. In addition, a custom 16 kB CMOS memory chip was designed to accept data from the converters. All chips except the memory were integrated on a custom thick film hybrid, shown in Figure 9. This system combined the strengths of three very different kinds of IC processes: GaAs for highest speed, bipolar for highest accuracy and CMOS for highest density of memory integration.

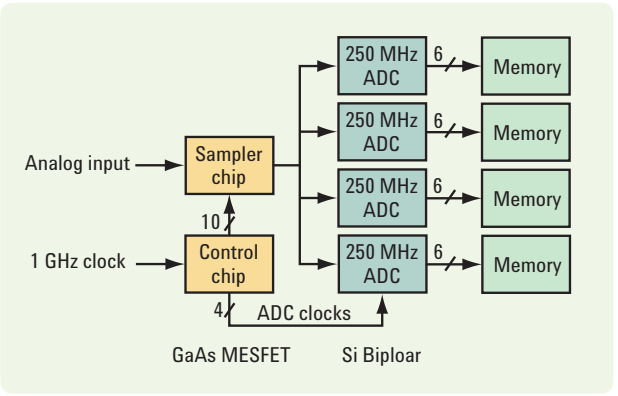


**Figure 8. Complete block diagram of 1 GS/s ADC system.**

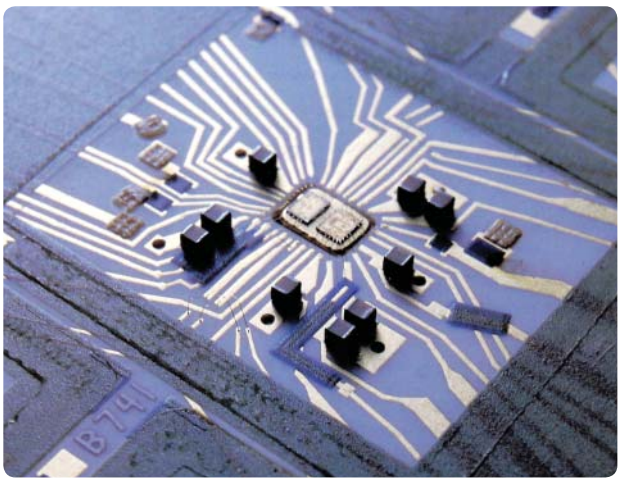

**Figure 9. Thick film hybrid package for 1 GS/s ADC system.**

Performance of the ADC system exceeded expectations. Analog bandwidth was 1.7 GHz, and 5.2 effective bits were achieved at 1-GHz input frequency and 1 GS/s[3]. The 54111D oscilloscope included numerous other significant technical achievements[4], and the product received strong acceptance in the marketplace.

## 1997: An 8-GS/s bipolar ADC system

The manufacturing cost of electronics does not change very much with the number of transistors in a chip, but is strongly related to the number of chips and the type of technology used in those chips. In the early 1990s, Agilent developed a world-leading 25-GHz-$f_T$ silicon bipolar process. Although it was an all-bipolar process, it was designed to take advantage of advances in CMOS lithography equipment to make many transistors with high yields. The high yield of the process offered the possibility of making a major step in complexity on a given chip, while reducing the chip count. The speed of the process offered the possibility of increasing the bandwidth and accuracy of the system while eliminating the more expensive GaAs chips.

The block diagram of this 8-GS/s system is shown in Figure 10. This system interleaves four bipolar digitizer blocks as in the 1-GS/s system; the sample rate of each one was increased by a factor of eight due to the faster process and circuit improvements. The resolution of each digitizer was increased from six bits to seven bits using an architectural feature known as interpolation; a combination of dither and a special digital filter increased the resolution at low input frequencies to eight bits. The higher process yield allowed higher complexity levels: increased resolution, on-chip preamp, digital with decimation logic, and putting two digitizers on a single chip. This reduced the chips in an acquisition channel from ten to four.

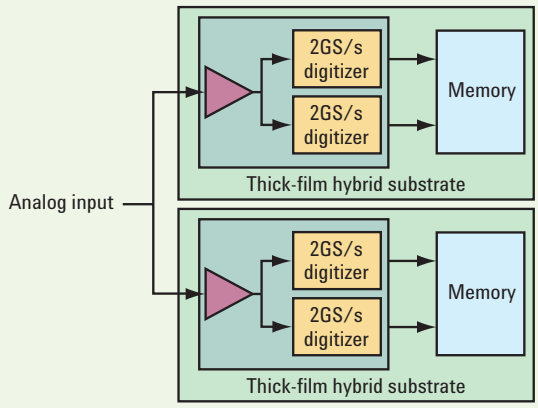


**Figure 10. Block diagram of the 4-chip 8-GS/s ADC system.**

This block diagram, however, has no single first-rank sampler, so it could suffer from time-interleaving errors at high input frequencies. The timing requirement is also eight times more stringent due to the higher input frequencies — up to at least 2 GHz. The solution came in the form of two inventions: programmable delay elements for the clock paths with picosecond resolution and stability, and algorithms to allow programmatic calibration of the delay elements.

The result is seen in Figure 11, showing the accuracy in effective bits versus input signal frequency. At low frequencies the DC accuracy of the ADC system is 6.7 bits. At higher input frequencies, the accuracy was reduced by distortion and jitter, but still provided the world's highest-accuracy ADC system for input signals above 1 GHz[5].

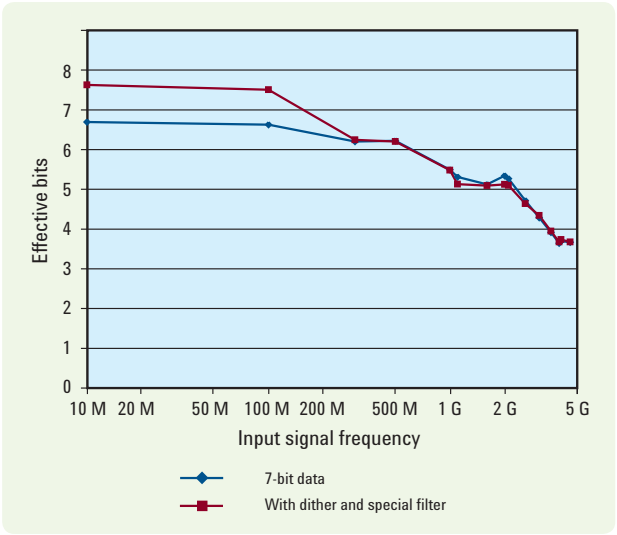


**Figure 11. Accuracy of the 8 GS/s ADC.**

## Today: The world's fastest ADC chip — in CMOS

In the late 1990s, CMOS processes were improving steadily, following Moore's Law, while bipolar process developments were improving less rapidly. We asked ourselves whether we could take advantage of the steady progress of CMOS.

At first, it seemed like a silly question. Existing 8-bit CMOS ADCs were 60 times slower than bipolar ADCs, and CMOS transistors are intrinsically about ten times less accurate than bipolar transistors. We came up with a radical departure from previous architectures to take advantage of the strengths of CMOS:

- Rather than building the fastest unit digitizer possible, we aimed at the most power-efficient unit digitizer. For 8-bit ADCs, CMOS pipelines are many times more power efficient (in gigasample/second/watt) than bipolar ADCs.
- We decided to run the pipelines at their most power-efficient speed and time-interleave as many pipelines as necessary to reach the required overall sample rate. This utilizes the biggest strength of CMOS: lots of transistors.
- We gave each pipeline converter its own input sampler connected directly to the analog input. The fastest clock signal used is only 1 GHz.
- To create the many very accurate sampling clocks required, we invented a clock generator using a delay-locked loop, dividers, and two levels of digitally-controlled delay circuits.
- For the pipeline digitizers, we chose an open-loop, current-mode circuit topology. Open loop circuits are generally faster than the more common feedback circuits, and current mirrors are more linear than the usual voltage amplifiers in CMOS.
- We made all the circuits as small as possible to reduce power, and relied on extensive calibration to make the overall conversion accurate. This uses even more transistors.

Our first CMOS ADC[6], initially shipped in oscilloscopes in 2002, replaced the 1997 4-GS/s bipolar ADC with a 4-GS/s, 8-bit CMOS ADC that used only one-third the power, and cost less than one-third as much, with better accuracy. This demonstrated the power of an architecture designed to fit the strengths of CMOS.

We then followed that with the world's fastest ADC in any technology: an 8-bit ADC at 20 GS/s[7]. To do this, we used a standard 0.18-micron CMOS process, built pipeline digitizers that ran at 250 MS/s, and time-interleaved an unprecedented 80 of these pipelines to reach 20 GS/s.

This ADC is used for input signals up to 13 GHz, which requires much higher bandwidth and much better timing accuracy than the bipolar converter operating on a 2-GHz signal. We addressed the bandwidth need by using carefully-optimized NMOS FET samplers. This is the only circuit in CMOS that can achieve 13 GHz bandwidth with the one percent linearity needed for scopes, so these samplers must be connected directly to the input pads. The resulting input capacitance (2 pF) is then driven from a small bipolar input buffer chip mounted in the same package as the CMOS ADC.

The last part of the puzzle is what to do with 20 GBytes/s of output data — about 100 times the write rate of a fast disk drive. We decided to take advantage of the integration capability of CMOS yet again and integrate the sample storage memory on the ADC chip. The resulting chip contains 50 million transistors; it is shown in Figure 12. The chip is dominated by the memory array in the bottom of the chip; the ADCs are in the upper portion. At the top is the separate input buffer chip.

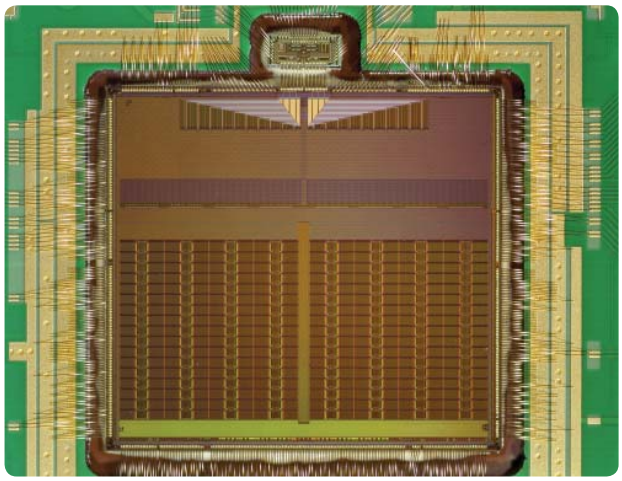

**Figure 12. 20-GS/s CMOS ADC chip**

Today's fastest Agilent oscilloscopes use one or two of these chips for each channel to reach sample rates up to 40 GS/s.

## Conclusion

What will the next 20 years bring in scope performance? CMOS technology is still moving forward and certainly will offer improvements in the performance of digital circuits. But the analog characteristics of CMOS devices are getting worse with CMOS scaling. Breakdown voltages and transistor gains are decreasing, and leakage currents are increasing, much to the detriment of analog circuits. On the other hand, carbon nanotubes or other device and process technologies may mitigate some of these problems. Alternatively, new circuit design approaches further exploiting redundancy or digital error correction may allow analog circuits to function well enough even with low yield or poorly functioning devices.

Will we see another 40 times improvement in ADC sampling rate (to over 1 THz) in the next 20 years? It seems unlikely. In fact, it seems just about as unlikely as 40 GS/s ADCs must have seemed to us in 1987.

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