6.1 A 1.2GS/s 15b DAC for Precision Signal Generation

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DAC sample rates over 1GHz with low spurious levels will enable new applications, particularly in signal simulation test equipment. Hundreds of MHz are needed in radar simulations, while predistortion in communication channels may require five times the nominal transmit bandwidth to cover 5th-order products, spreading out to over 100MHz. This circuit was designed to meet the simultaneous requirements of very wide signal bandwidth and high dynamic range.

In Fig. 6.1.1, two data ports at 600MS/s are multiplexed together for a 1200MS/s data stream. The nine LSBs switch nine unit current sources to the taps of a differential R/2R ladder. The six MSBs are decoded into 64 current request signals which are pseudo-randomly scrambled for dynamic element matching (DEM) of the 64MSB unit currents, which are added to the output of the R/2R ladder. In optional modes, a single port can accept data at up to 1200MS/s and the DEM can be disabled to allow a trade-off between DNL and noise. The input receivers accept either LVDS- or ECL-level signals at 1200MHz. MOS source followers level shift the inputs to a more positive common-mode voltage, and the signal is then applied to a bipolar differential pair.

For data alignment, the on-chip data phase detector generates an early/late indication of whether the internal latch clock is centered in the data eye. The early/late data phase detector is similar to a design by Alexander[1]. A separate input flip-flop is clocked with a 180-degree clock at the data transition. If the data captured before and after that transition are different, the out-of-phase flip-flop will indicate whether the transition was early or late. The indications are latched on the DAC to allow timing adjustment by the data source.

To improve INL and DNL, dynamic element matching of the 64MSB current sources is used. The eight least-significant current request lines, which include the three least-significant MSBs and an extra bit from the LSBs, are applied to one eight-way barrel shifter which is controlled by three pseudo-random bits. The eight output lines for those less-significant MSBs are fanned out, one each to eight additional eight-way barrel shifters, which have as their additional 56 inputs the values of the top three MSBs weighted in the ratio of 8:16:32 to match their significance. Three more pseudo-random bits control the second tier of shifters. Each current source is thus used an equal fraction of the time for any particular input code. The pseudo-random controls are generated from multile delays of a 1b pseudo-random (PR) sequence that comes in as a 16th bit with the data.

Any mismatch or skew in the timing of either the switching of the current sources or the arrival of the currents at the output results effectively in jitter when DEM is in use or in non-linearity otherwise. For deglitching and precise time alignment of the current switching, resampling allows the data-selected current to settle before it is connected to the output. A single series switch for all of the output current was not linear enough for the target performance, so the resampling is done separately for each current source as shown in Fig. 6.1.2. The unit current source is an NPN transistor with a tail resistor. The data pair switches the current to the left or right upper pair, which are the resamplers, at the start of the clock cycle. During settling, the current is dumped to the positive rail and is then switched to the output R/2R ladder, which is referenced to the positive rail. Since each unit current source has its own output resampler, the linearity of the resampling devices versus the current they are passing is not important [2]. The output waveform after resampling is return-to-zero (RZ) with zero current between the resample times. This reduces the $\sin(x)/x$ roll-off versus a non-return-to-zero (NRZ) waveform, but for better SNR below the Nyquist frequency, a second set of current sources and switches was included. This produces the same RZ waveform delayed by half a clock cycle, the sum gives an NRZ result.

The 5.2×5.9mm² chip, made with 40GHz f_t NPNs and 0.35µm CMOS, is shown in Fig. 6.1.3. The largest features visible are the tail resistor arrays which used a common-centroid structure and were sized for negligible contribution to current-source mismatch compared to the transistor mismatches. The package is a 256-pin ball-grid array. The chip uses 1.6A from the 3.3V main supply and about 110mA from the V_{REF} supply for a total dissipation of about 6W.

Figure 6.1.4 shows the worst-case harmonic versus signal frequency for 1200MHz and 500MHz clocks. At 1200MS/s, harmonics remain below -70dBc up to $f_s/4$ and under -63dBc up to Nyquist, while for the reduced-rate clock, the corresponding harmonic levels are -83dBc and -74dBc respectively.

Figure 6.1.5 shows the noise spectral density (NSD) versus clock rate for a typical chip measured in each case near $f_s/4$. For low clock rates, there is an increase of 3dB/octave as the frequency is reduced, due to a constant RMS noise (from fixed mismatches) in a decreasing Nyquist bandwidth. As the clock rate is increased, a floor is reached at -161dBc/Hz and at a 1200MHz clock rate, it is -159dBc/Hz. The chip operates correctly up to 2000MS/s, but testing was very limited above 1200MHz due to the lack of a suitable data source. INL is shown in Fig. 6.1.6 with DEM off and on. The DNL is improved by over a factor of 3 typically with DEM, but the overall INL acquires a strong third-order component due to switching transients around the data pairs in the current sources.

When the resampling switches are disabled, and the current flows continuously from the data switches to the output, performance on a typical test is degraded by about 6dB. A major benchmark for testing is with a multi-carrier wide-band signal, such as WCDMA. With four occupied 5MHz channels at around 300MHz, the typical ACPR (adjacent channel power ratio) was 73dB for a signal crest factor of 14.7dB. Direct generation in a cellular phone band at 900MHz ($3f_s/4$) is shown in Fig. 6.1.7. With a reduced crest factor of about 8dB, the measured ACPR was 69dB.

References:

[1] J. D. H. Alexander, "Clock Recovery from Random Binary Data," Elect. Lett., vol.11, pp 541-42 Oct., 1975,

[2] R. Jewett and J. Liu, "Per-Element Resampling for a Digital-to-Analog Converter," U.S. Patent 6812878, Nov., 2004.

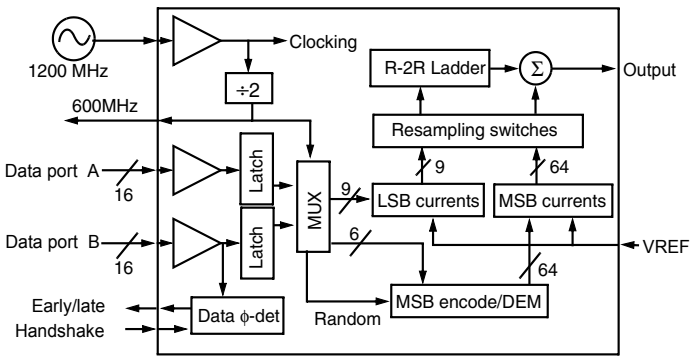

Figure 6.1.1: DAC Block Diagram.

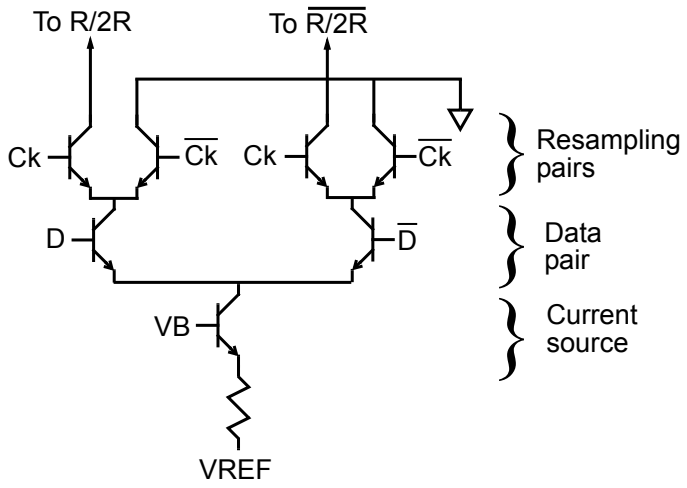

Figure 6.1.2: Current source resampling.

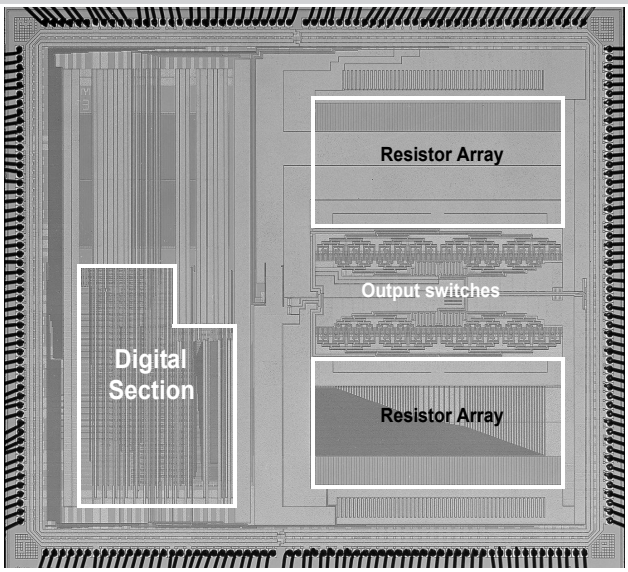

Figure 6.1.3: Die micrograph.

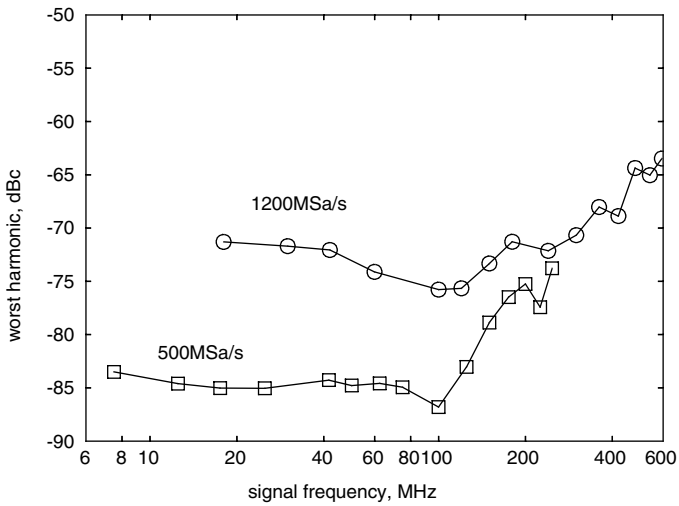

Figure 6.1.4: Worst harmonic versus signal frequency, fs as a parameter.

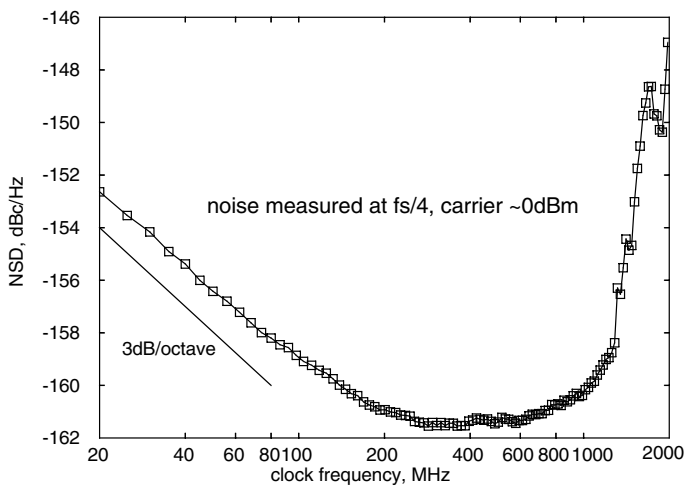

Figure 6.1.5: Noise spectral density versus clock rate.

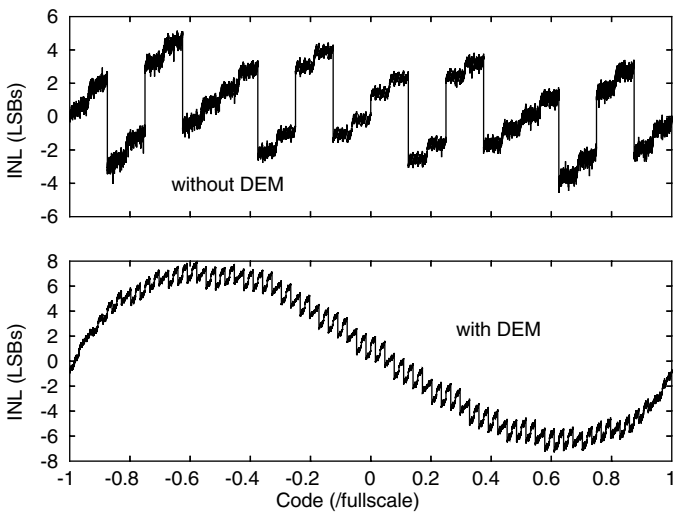

Figure 6.1.6: INL with and without DEM.

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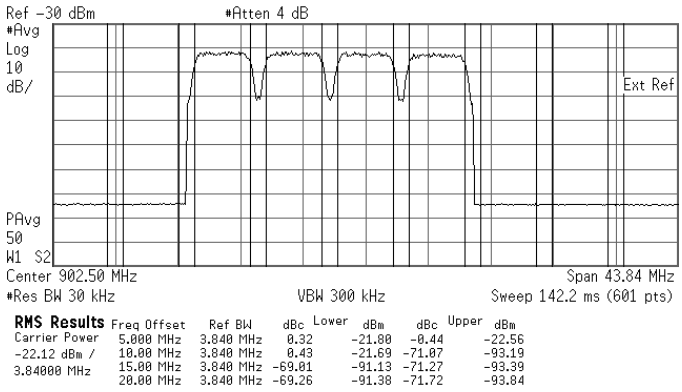

Figure 6.1.7: ACPR for 20MHz bandwidth at 900MHz.

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