BANDWIDTH AND BITS: NEW AWG DESIGN ACHIEVES BOTH

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Abstract - This paper describes the architecture and application of a new modular dual arbitrary waveform generator (AWG) capable of generating 1 GHz of modulation bandwidth and over 65 dB of spurious-free dynamic range (SFDR). The key technology consists of two Agilent-developed digital-to-analog converters (DAC) operating at 1.25 gigasamples per second (GSa/s) clock frequency with 15 bits of vertical resolution. The new design supports advanced waveform sequencing and triggering for event-based pulse building. This new level of performance gives designers the ability to generate not only wide-bandwidth pulse compression radar signals, but also to add interfering radar and EW signals into the signal scenario. When combined with wide-bandwidth IQ and pulse modulators, real-world signatures can be realized at microwave frequencies.

INTRODUCTION

Wideband signal simulators are employed in many modern military and commercial systems. The use of wideband signals offer improvements in spatial resolution, target information recovery, detectable materials penetration and lower probability of intercept compared to narrowband signals [1].

Signal simulators are often utilized during the design phase to evaluate system and subsystem performance. At the heart of these test systems is frequently an arbitrary waveform generator (AWG) capable of synthesizing clean, wide-bandwidth waveforms. Such signals are a challenge to realize with commercially available AWGs, as they tend to offer either high sampling bandwidths or high spurious-free dynamic range, but not both, simultaneously. System designers then have two

fundamental choices in realizing these real-world signals. The first is to spend the required time and money to create a custom AWG from commercially available digital-to-analog converters (DAC). This approach affords the designer the opportunity to optimize the AWG design by including extra sample memory or triggering I/O required by the simulator. However, this approach defocuses their primary role of designing more value-added system elements. The other approach is to invest in simulation hardware in the form of a "golden radio". Besides the incremental investment in building a dedicated signal generator, calibration, traceability and support costs become important issues for systems where up-time is critical.

With the recent advances in DAC and digital signal processing (DSP) technology, high performance AWGs can be created to simplify the designer's efforts and reduce schedule risk in mission critical applications. This paper describes the architecture and application of a new modular dual AWG capable of generating signals with 1 GHz of modulation bandwidth with over 65 dB of spurious-free dynamic range. Key to the design are two Agilent-developed DACs operating at 1.25 GSa/s clock frequency with 15 bits of vertical resolution. The new AWG design supports advanced waveform sequencing and triggering for event-based pulse building, more efficiently using the waveform memory. This new level of performance gives designers the ability to generate not only wide-bandwidth pulse compression radar signals, but also to add interfering radar and EW signals into the signal scenario. When combined with a wide-bandwidth IQ and pulse modulators, real-world signatures can be realized at microwave frequencies.

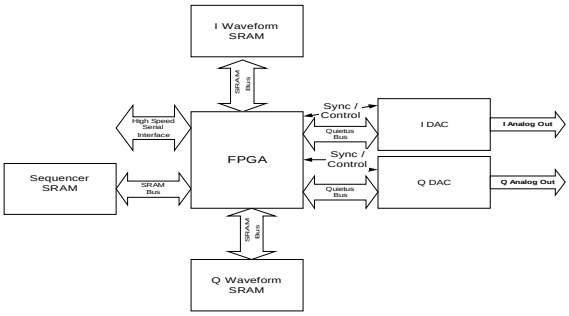
SYSTEM OVERVIEW

Figure 1 highlights the core functional blocks of the AWG design. The AWG has two independent, differential outputs that are controlled by a memory sequencer. The sequencer allows efficient use of the memory with several levels of nested loops. The Xilinx Virtex-II Pro FPGA multiplexes data from the SRAM memory over an LVDS interface to two Agilent-developed high-speed DACs. The Virtex-II Pro FPGA was chosen as it uniquely provides a combination of: a large number of I/O pins to interface to the SRAM and dual DACs, a high-speed serial interface for data transfers and a sophisticated reconfigurable core for DSP functions. Synchronization of the two DAC outputs is achieved by distributing common clocks and triggers. This same synchronization control also allows for system scaling so multiple generators can be triggered; all with repeatable skew. The high-speed serial interface is a real-time data port based on Xilinx's RocketIO™ interface design and is capable of sustained data transfer rates in excess of 1.25 GSa/s.

Operation with both an internal or external sample clock is supported. In addition to the sequencing and multiplexing functions, the FPGA also allows higher-level DSP functionality such as FIR filters. The analog outputs are conditioned with reconstruction filters to suppress aliasing products.

The AWG was realized in a 3U CompactPCI module because of its compact size, efficient system scaling and reliance on an open industry standard. This form-factor also allowed the designers focus on value-added design elements of the DAC, DSP and analog sections.

Figure 1. Dual AWG Block Diagram



DAC TECHNOLOGY

The DAC chip was developed at Agilent Laboratories, Agilent's long-term R&D center in Palo Alto, California. R&D within each of Agilent's product divisions is largely focused on the next product introduction, so Agilent Laboratories takes a complementary role, focusing on riskier and longer-term projects.

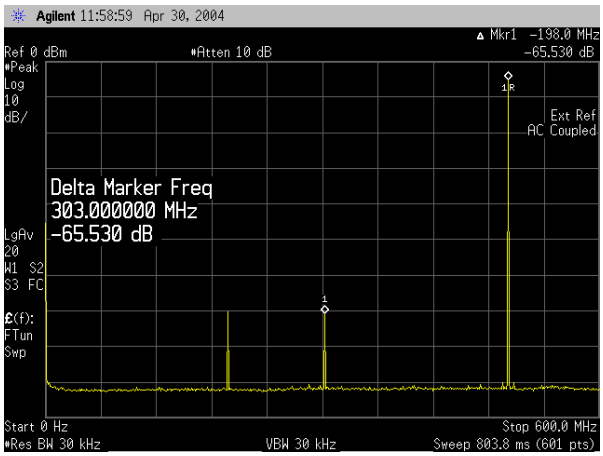
The DAC was designed to achieve the highest possible spurious-free dynamic range (SFDR) and adjacent-channel power ratio (ACPR) for signals with analog bandwidths up to 500 MHz. The DAC's design was implemented in a SiGe BiCMOS process for high speed and supports a sample rate of 1.25 GSa/s. To ease the burden on the digital circuits providing the data, it can accept data on one parallel LVDS port at the full clock rate, or on two ports at half the DAC clock rate. The DAC has 15 bits of resolution to ensure that quantization noise is negligible.

A key element of DAC performance is avoiding nonlinearity due to current source mismatch. The Agilent DAC starts with current sources that are matched to better than 0.1% by careful design. However, this is insufficient for high-performance RF signals. The DAC also uses dynamic element matching – choosing a different set of current sources at each clock cycle, even if the input code value is the same. This averages out any remaining mismatch. Nonlinearity due to mismatch is converted into a low level of white noise, while harmonics and spurs are greatly reduced.

Another critical aspect of DAC performance is maintaining high linearity at high output signal frequencies. This DAC does that with a resampling structure that "throws away" the nonlinear settling part of each output current pulse and passes only the settled portion. In this way, each pulse has the same clean "on" and "off" transition. Agilent invented a new way to implement resampling that avoided limitations of the existing methods.

The result is SFDR, which is better than 70 dB up to 360 MHz signal frequency and better than 65 dB up to 500 MHz. Figure 2 shows the output spectrum with a 501 MHz signal.

Figure 2. AWG Output Signal Performance from a 501 MHz Tone



DSP DESIGN

To compliment the high speed and wide dynamic range of the DACs, the Agilent AWG includes real-time signal processing capable of supporting the full GHz of available signal bandwidth. The DSP engine can be used to correct for imperfections localized in the AWG (frequency dependant gain variations, zero-order-hold roll-off, I/Q group delay skew, non-linear group delay) but can also be applied to channel impairments in the analog and RF hardware downstream of the AWG. For RF/Microwave systems employing an analog I/Q modulator, these corrections can significantly reduce the magnitude of unwanted images. The performance enhancements from real-time DSP are applicable to both memory-based waveform data and applications requiring streaming data from an external source. For applications where zero padding the waveforms is acceptable, the corrections could be applied to the stored data. This option is not limited by the complexity of real-time correction filters and may be the preferred approach for some applications.

Figure 3. Modeled Improvements in Real-Time Corrections on Complex DAC Data

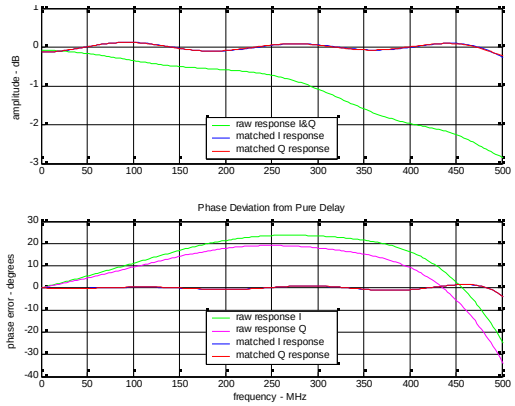
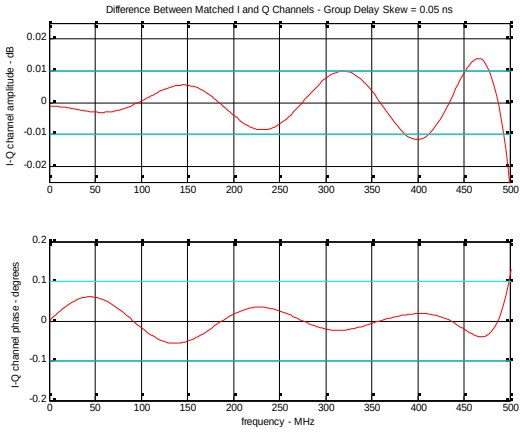


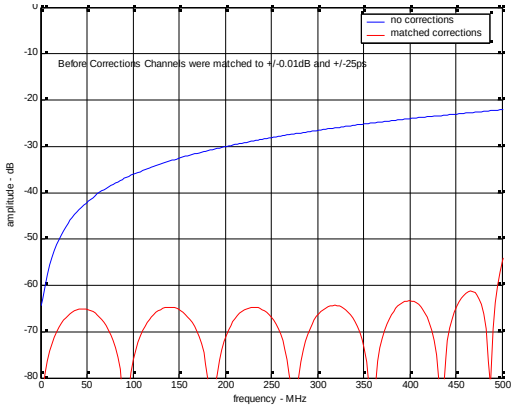
Figure 3 highlights simulation results of the improvements expected for real-time corrections on complex data. Channel impairments include 7th order reconstruction filters and up to 50 picoseconds of timing skew between I and Q channels. The result shows that both channels are flattened to within +/- 0.1dB and phase linear to +/- 2° up to 480 MHz, slightly more up to the targeted bandwidth of 500 MHz (0.8*Nyquist). Channel matching is very important for image performance. The corrections also employed a channel matching optimization algorithm and was successful in achieving +/-0.014 dB and +/-0.06° up to 480 MHz. The results of the channel matching simulation are shown below in Figure 4.

Figure 4. Channel Matching Performance



The resulting image levels (Figure 5) are quite impressive, far exceeding the performance one would expect from an analog system without the advantages of the high sample rate real-time corrections. It's important to note that, with proper calibration, the correction-processing engine can also correct impairments in the system the AWG is driving. This adds value to the overall system performance and may be the most cost effective way to add bandwidth and increase the system precision.

Figure 5. Image Performance of Raw and Corrected Channels



Additional DSP type functions are possible and are being explored. These include nonlinear corrections to improve spurious performance.

SEQUENCING ENGINE

The AWG also contains an advanced sequencer to allow the user to address waveforms stored in RAM in several modes. There are three main components to the sequencer:

Waveform Address Generator

- Produces addresses for the waveform RAM
- Handles waveform looping
- Responds to jump triggers

Packet Memory Controller

- Interfaces to the packet RAM
- Supports packet advance modes and looping
- Responds to triggers

Play List Controller

- Accesses the sequence play list
- Host interface allows random access to sequences

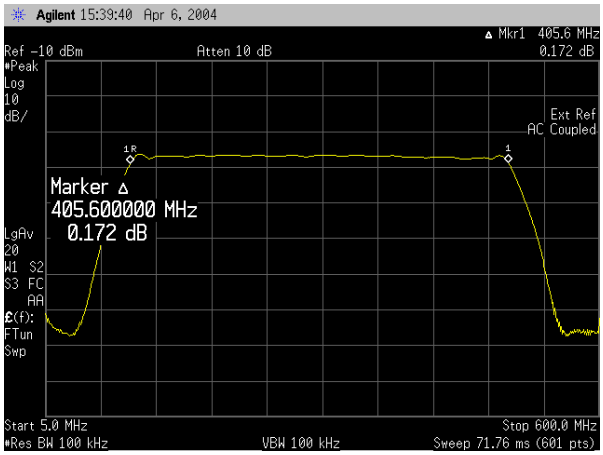
These main blocks provide a flexible environment for user access to the stored waveform and sequence data. The various looping and advance modes allow the user to effectively compress the waveforms and sequences, greatly extending the effective record length. The sequencer is designed to have the shortest possible latency in response to a trigger or command from the external host. The sequencer clock runs at 1/8th of the clock rate of the DACs. External triggers and host commands are synchronized to the sequencer clock and will have repeatable latency. For lower bandwidth applications, waveform samples can be repeated by a programmable number of samples. This increases the effective length of the time record but does not degrade noise performance, since the DACs continue to operate at the original sample rate.

Marker information can be stored in the waveform RAM (high resolution), in the packet memory or in the play list (both at 1/8th DAC clock resolution). Marker mask bits allow the user to configure the markers functionality. Triggers can be applied externally or through the host interface.

WIDEBAND APPLICATION

Figure 6 below show an example of a wideband waveform generated using the new AWG. The signal utilizes pulse compression generated from linear frequency modulation chirped at 400 MHz/us. Such signals are frequently used in radar applications to maximize range resolution from short pulses [2]. The pulse was constructed in MATLAB® and played using one of the AWG's two independent output channels. The pulse was pre-distorted for amplitude and phase flatness to correct for sinc roll-off. Such wideband signals are useful as the IF stimulus in receiver test or applications aimed at performance verification of transmitter up-converter subsystems. Multi-emitter scenarios can also be constructed in MATLAB®, downloaded to the AWG for more complex signal simulations. Ultra wideband signals can be realized using both channels of the AWG. For example, utilizing the 500 MHz bandwidth on each channel, the AWG can drive the IQ inputs of a vector signal generator to create chirps covering a full GHz of spectrum. Alternately, narrower-band signals created using this AWG-vector generator combination can hop at nanosecond rates.

Figure 6. Radar Chirp at 400 MHz/us - 1.25GSa/s Clock



SUMMARY

Agilent's new modular AWG design enables a breakthrough in high-fidelity wideband signal generation. The prototype has shown more than 65 dB of SFDR across a 500 MHz bandwidth on each of the AWG's analog outputs. Its sequencing engine extends total waveform playtime through its waveform looping and multiple advance modes. The AWG can be used as a building block for IF and RF subsystems, or as a wideband stimulus for vector signal generators.

References

[1] Taylor, James D., *Introduction to Ultra-Wideband Radar Systems*, CRC Press, 1995, pp. 1-7.

[2] Skolnik, Merill I., *Introduction to Radar Systems*, McGraw Hill, 1980, pp 420-434.