A 4 GSample/s 8-bit ADC in 0.35 μm CMOS

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Outline

■ Background
■ Chip Architecture
■ Key Circuits
  ● Interleaved Clocks
  ● Front-end Track/Hold
  ● ADC
  ● Digital Circuits
  ● Calibration
■ Results
■ Summary
Application: Digital Oscilloscopes

- Real time waveform acquisition
  - Maximum sample rate
  - Inputs band-limited to $\sim \frac{F_{\text{sample}}}{4}$
  - $\sim$ 8 bit resolution
- External CPU and calibration sources

ADC Designer’s ‘scope block diagram
Design Goals

- Goals:
  - 4 GSample/s, 8 bit conversions
  - 7 effective bits (ENOB) at low frequency
  - > 5 ENOB at $F_{\text{in}}=1$ GHz ($F_s/4$)
  - -1 dB bandwidth of 1 GHz.
  - Low enough power for standard packaging

- Approach:
  - Use time-interleaved ADCs to get high sample rate
  - Minimize the high-speed analog signal path
  - Make all the circuits small for low power
  - Take full advantage of offline calibration
ADC Chip Architecture

- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s
Background: Timing Error and ADC Resolution

- Fast signal converts a sample timing error ($dT$) to an apparent voltage error ($dV$).
ADC Effective Bits vs Timing Error

- Rule of thumb: 1 ps / 1 GHz --> 7 effective bits
Clock Timing Errors

■ Cycle/Cycle Errors (jitter)
  ● Thermal noise induced jitter
  ● Substrate and supply noise induced jitter

■ Static Errors
  ● Clock and signal path mismatches (time of flight)
  ● Device and parasitic mismatches

■ Design Approach
  ● Shorten total clock delay to reduce errors.
  ● Calibrate remaining static errors.
Direct Approach: 31 Stage DLL

31 stages, 250 ps/stage, total delay 8 ns

To Track/Hold Circuits

- Static timing errors: Error \sim total delay
- Supply noise coupling: Error \sim total delay
- Thermal jitter: Power \sim (total delay)^2

DLL meeting jitter spec would consume entire ADC power budget!!
Timing Generator

- Max input edge to sampling edge delay: 2 ns
- ~ 1 ps jitter
- < 1 ps static error after cal
Simplified Input Track/Hold

To achieve highest bandwidth and linearity:

- **ONLY** 1 NMOS FET in signal path
- Restrict $C_{\text{hold}}$ to only T/H and load parasitics
- Low common mode input voltage
- Low-swing differential signal (250 mV peak)
- Fastest possible full-swing clock edge

2 GHz bandwidth, -50 dB HD3 at 1 GHz
Interleaved Track/Hold Input Circuits

Requirements

- 2 GHz input bandwidth to $C_{\text{hold}}$
- Low parasitics on $V_{\text{in}}$
- Kickback to $V_{\text{in}}$ must be independent of signal

32 T/H Circuits (125 MSa/s)
Analog Front End Implementation

- Parasitic-only hold capacitance (140 fF)
- Only 1 ns pulse width for Clk_s
- Reset phase
- Transconductor (V/I) current output drives ADC
### 125 MSa/Sec 8-bit Full Nyquist ADC

<table>
<thead>
<tr>
<th>Key Attribute</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pipelined Architecture</td>
<td>Low power</td>
</tr>
<tr>
<td></td>
<td>Small area</td>
</tr>
<tr>
<td></td>
<td>Low input capacitance</td>
</tr>
<tr>
<td>1 bit / Stage</td>
<td>Highest speed pipeline</td>
</tr>
<tr>
<td>Open-loop amplifiers</td>
<td>Fastest settling</td>
</tr>
<tr>
<td>Current mode signals</td>
<td>No explicit capacitors</td>
</tr>
<tr>
<td>(Switched current mirrors)</td>
<td>Small Area</td>
</tr>
<tr>
<td>Scale for thermal noise</td>
<td>Smallest area and power</td>
</tr>
</tbody>
</table>

### Making it work

<table>
<thead>
<tr>
<th>Making it work</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduce Radix to 1.6</td>
<td>Achieves Redundancy</td>
</tr>
<tr>
<td>Digital Calibration</td>
<td>Corrects amplifier gain and offset errors.</td>
</tr>
</tbody>
</table>
Pipeline ADC Block Diagram

Corrected Output (8 bits, binary)

Radix Conversion Circuit

Raw ADC output: 12 bits, Radix 1.6

De-skew latches

Input

1-bit quantizer

Clock

1

1-bit quantizer

2

1-bit quantizer

12

Input

T/H

Clock

Residue

G=1.6

FF

G

DAC

● Only 1 comparator per stage

Radix Conversion Circuit

G=1.6

Corrected Output (8 bits, binary)

Radix Conversion Circuit

G=1.6

Corrected Output (8 bits, binary)
Good Linearity: Current mirrors with cascodes are 8 bit linear.

Poor Accuracy: Gain and offset errors
Current-Mode ADC Stage

Gain = 1.6
Current-Mode Pipeline ADC

- State of the art speed/power ratio for an 8-bit ADC
  - 125 MSa/s, full nyquist performance
  - 80 mW total
    - 20 mW V/I buffer
    - 40 mW pipeline
    - 20 mW radix converter

- Small Area
  - 0.3 mm$^2$
Radix Converter - Principle of Operation

Calculate and download bit weights during cal.

Output = \( b_{11} \cdot w_{11} + b_{10} \cdot w_{10} + \ldots + b_1 \cdot w_1 + b_0 \cdot w_0 \)

- Look-up table is an alternative.
- This ADC uses a hybrid look-up/adder.
Supply and Substrate Noise Reduction

- Fully differential analog path
- Very low-noise digital logic family (SCL - Source Coupled Logic)
  - Differential Logic
  - Constant Supply Current
  - Generates less noise than the ADC Comparators!!
- Differential output drivers
- Chip-level supply and substrate noise simulation for design verification.
What Needs To Be Calibrated?

- Offline Calibration with DC and Pulse sources

Clocks

- DLL
- Clock Gen
- 32 T/H+V/I
- 32 ADCs
- 32 RCs
- Per-slice Gain + Offset DACs
- RC Bit Weights
- External Lookup Table

Radix Converters

Timing Adjust
Offline Calibration

■ DC Linearity Calibration
  ● Use a DC ramp input, observe ADC radix bits
  ● Analog gain and offset trim per path
  ● Use least squares fit on a large record to find optimal bit weights and 3rd harmonic fit.
  ● Least squares fit minimizes INL

■ Timing Calibration
  ● Apply a pulse train with fast edges
  ● Use an FFT to measure phase delay on each T/H
  ● Adjust time delays, and iterate

Full ADC calibration takes about 3 minutes
ADC 256-Ball TBGA Package

- Copper body
- Controlled-impedance lines
- Custom layout, standard ball pattern
Acquisition Before Calibration

~ 5 effective bits
Acquisition With Calibration

$F_s = 4000 \text{ MSa/sec} \quad F_{in} = 30.27 \text{ MHz} \quad 7.0 \text{ effective bits}$
Acquisition With Calibration

F_s = 4000 MSa/sec   F_in = 30.27 MHz   7.0 effective bits

Equivalent Time (ns)

Noise: 0.6 LSB rms
Full Calibration, With 1 GHz Input

\[ F_s = 4000 \text{ MSa/s} \quad F_{\text{in}} = 1026.4 \text{ MHz} \quad 6.35 \text{ effective bits} \]
Static Linearity

INL (LSBs)

DNL (LSBs)

raw INL

with Lookup table

ADC code
ADC Effective Bits vs Input Frequency

Accuracy (Effective Bits)

Frequency (Hz)

Input amplitude ~95% of full scale

1.2 ps rms clock error
ADC Amplitude Response

-1 dB at 1.3 GHz     -3 dB at 1.6 GHz

Input Frequency (Hz)

Amplitude Response (dB)
## ADC Chip - Key Specs

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Nominal Sample Rate</strong></td>
<td>4</td>
<td>GSa/s</td>
</tr>
<tr>
<td><strong>Sample Rate Range</strong></td>
<td>0.1 - 5.9</td>
<td>GSa/s</td>
</tr>
<tr>
<td><strong>Resolution</strong></td>
<td>8</td>
<td>bits</td>
</tr>
<tr>
<td><strong>3 dB Bandwidth</strong></td>
<td>1.6</td>
<td>GHz</td>
</tr>
<tr>
<td><strong>Accuracy</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 MHz</td>
<td>7.0</td>
<td>effective bits (ENOB)</td>
</tr>
<tr>
<td>1 GHz</td>
<td>6.2</td>
<td></td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>0.6</td>
<td>LSB rms</td>
</tr>
<tr>
<td><strong>INL / DNL</strong></td>
<td>±0.3 / ±0.2</td>
<td>LSB</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>4.6 W at 3.3 V</td>
<td></td>
</tr>
<tr>
<td><strong>IC Technology</strong></td>
<td>0.35 μm CMOS</td>
<td></td>
</tr>
<tr>
<td><strong>Chip Size</strong></td>
<td>7.14 x 4.04 mm²</td>
<td></td>
</tr>
<tr>
<td><strong>Transistors</strong></td>
<td>300,000</td>
<td></td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>256 ball TBGA</td>
<td></td>
</tr>
</tbody>
</table>
Monolithic ADCs

This work
Summary

■ Features:
  ● Interleaving of 32 ADCs
  ● Precision timing generator for 32 clock phases
  ● Current-mode pipeline provides a superior speed/power ratio
  ● Extensive calibration to achieve accuracy

■ Results:
  ● 2x lower power/Gsample than any reported GSa/s 8-bit ADC
  ● Highest reported clock rate for 6-8 bit CMOS ADCs
  ● Highest reported accuracy at 4 GSa/s