A 4 GSample/s 8-bit ADC in 0.35 μm CMOS

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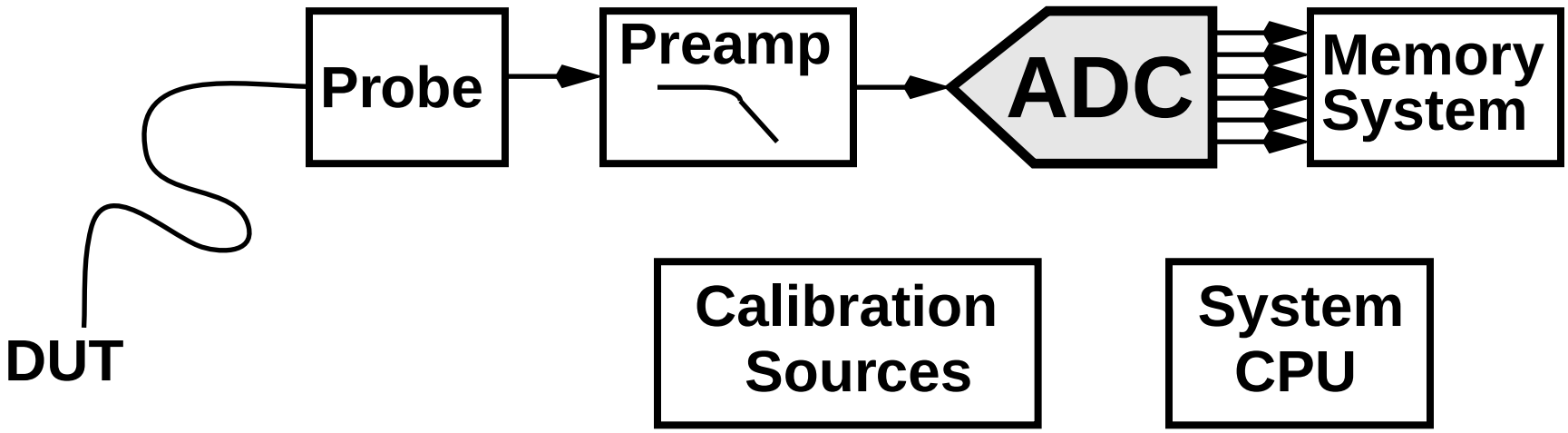
Outline

- Background
- Chip Architecture
- Key Circuits
  - Interleaved Clocks
  - Front-end Track/Hold
  - ADC
  - Digital Circuits
  - Calibration
- Results
- Summary

Application: Digital Oscilloscopes



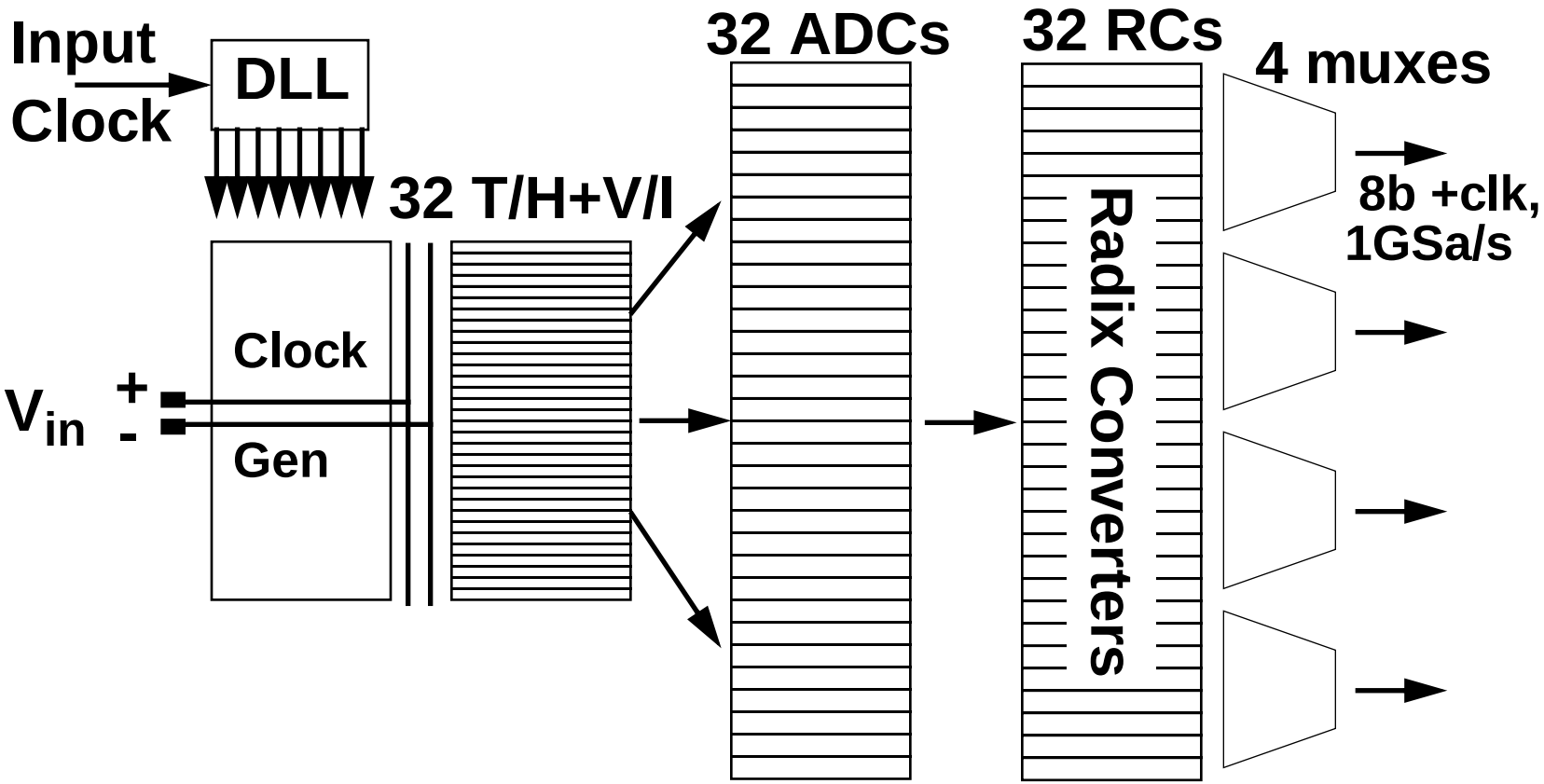
ADC Designer's 'scope block diagram

- Real time waveform acquisition
  - Maximum sample rate
  - Inputs band-limited to ~ $F_{sample}/4$
  - ~ 8 bit resolution
- External CPU and calibration sources

Design Goals

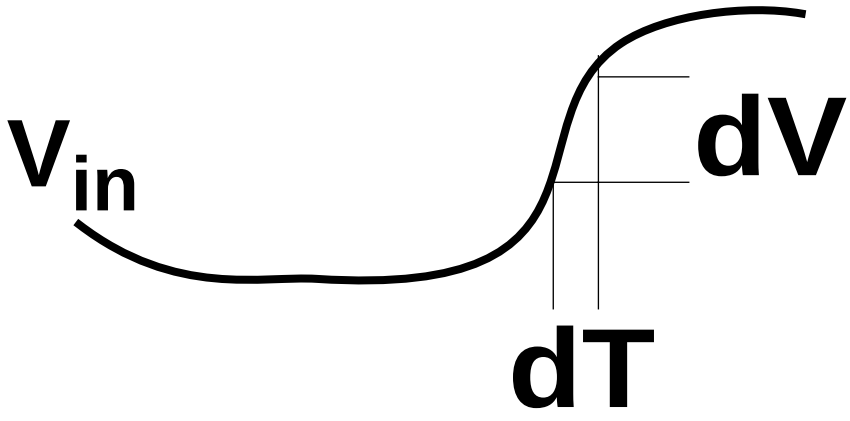
- Goals:
  - 4 GSample/s, 8 bit conversions
  - 7 effective bits (ENOB) at low frequency
  - > 5 ENOB at F_{in}=1 GHz (F_s/4)
  - -1 dB bandwidth of 1 GHz.
  - Low enough power for standard packaging
- Approach:
  - Use time-interleaved ADCs to get high sample rate
  - Minimize the high-speed analog signal path
  - Make all the circuits small for low power
  - Take full advantage of offline calibration

ADC Chip Architecture



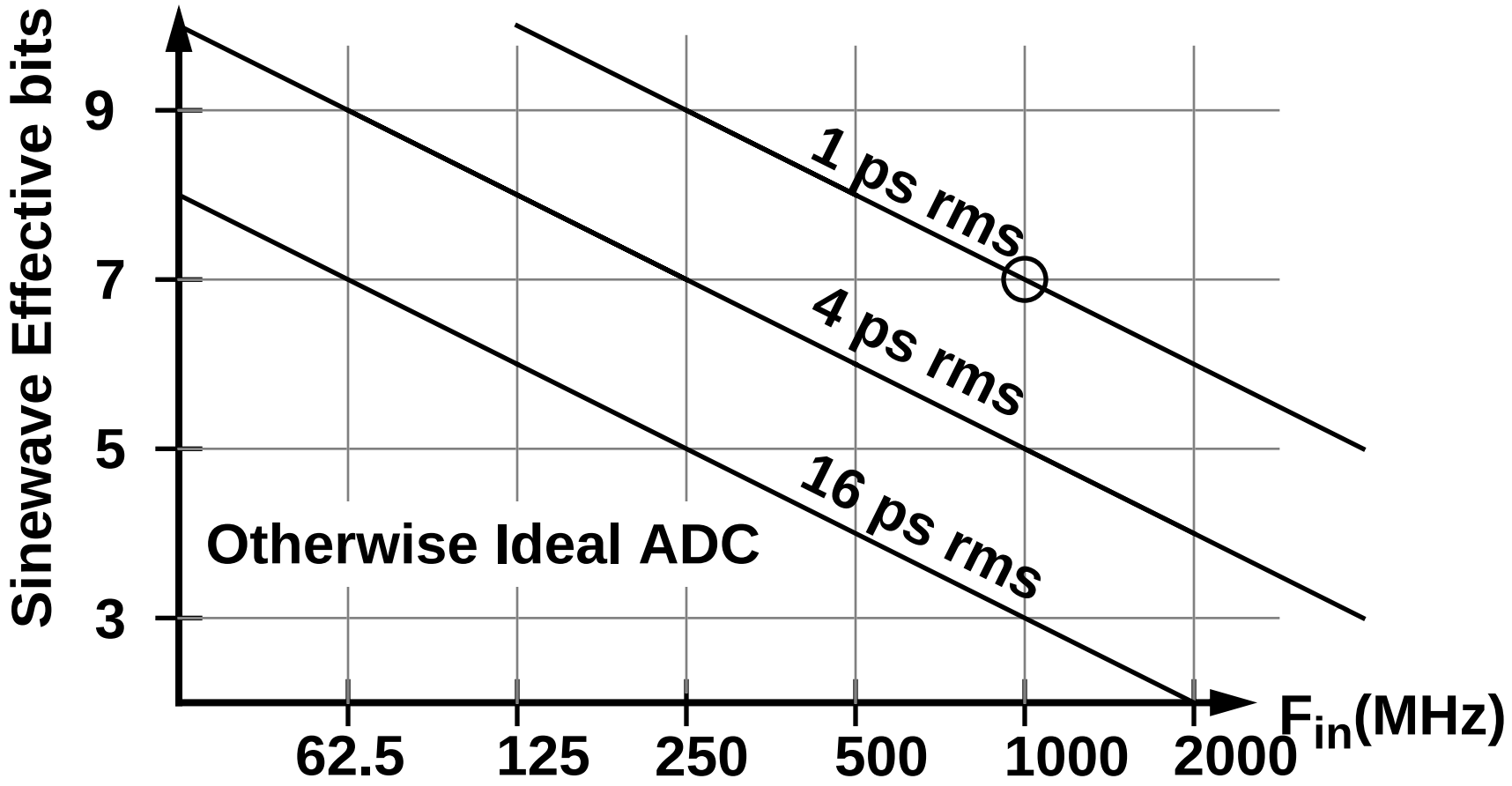
- 32 time-interleaved pipeline ADCs at 125 MSa/s
- Net sample rate is 4 GSa/s

Background:
Timing Error and ADC Resolution



- Fast signal converts a sample timing error (dT) to an apparent voltage error (dV).

ADC Effective Bits vs Timing Error

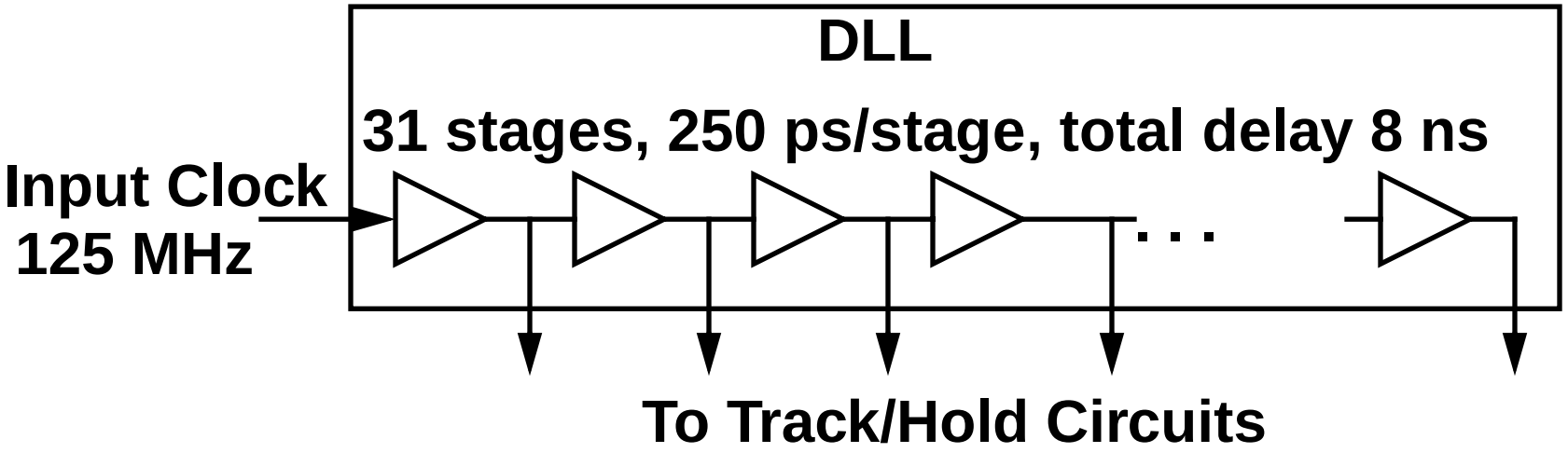


- Rule of thumb: 1 ps / 1 GHz --> 7 effective bits

Clock Timing Errors

- Cycle/Cycle Errors (jitter)
  - Thermal noise induced jitter
  - Substrate and supply noise induced jitter
- Static Errors
  - Clock and signal path mismatches (time of flight)
  - Device and parasitic mismatches
- Design Approach
  - Shorten total clock delay to reduce errors.
  - Calibrate remaining static errors.

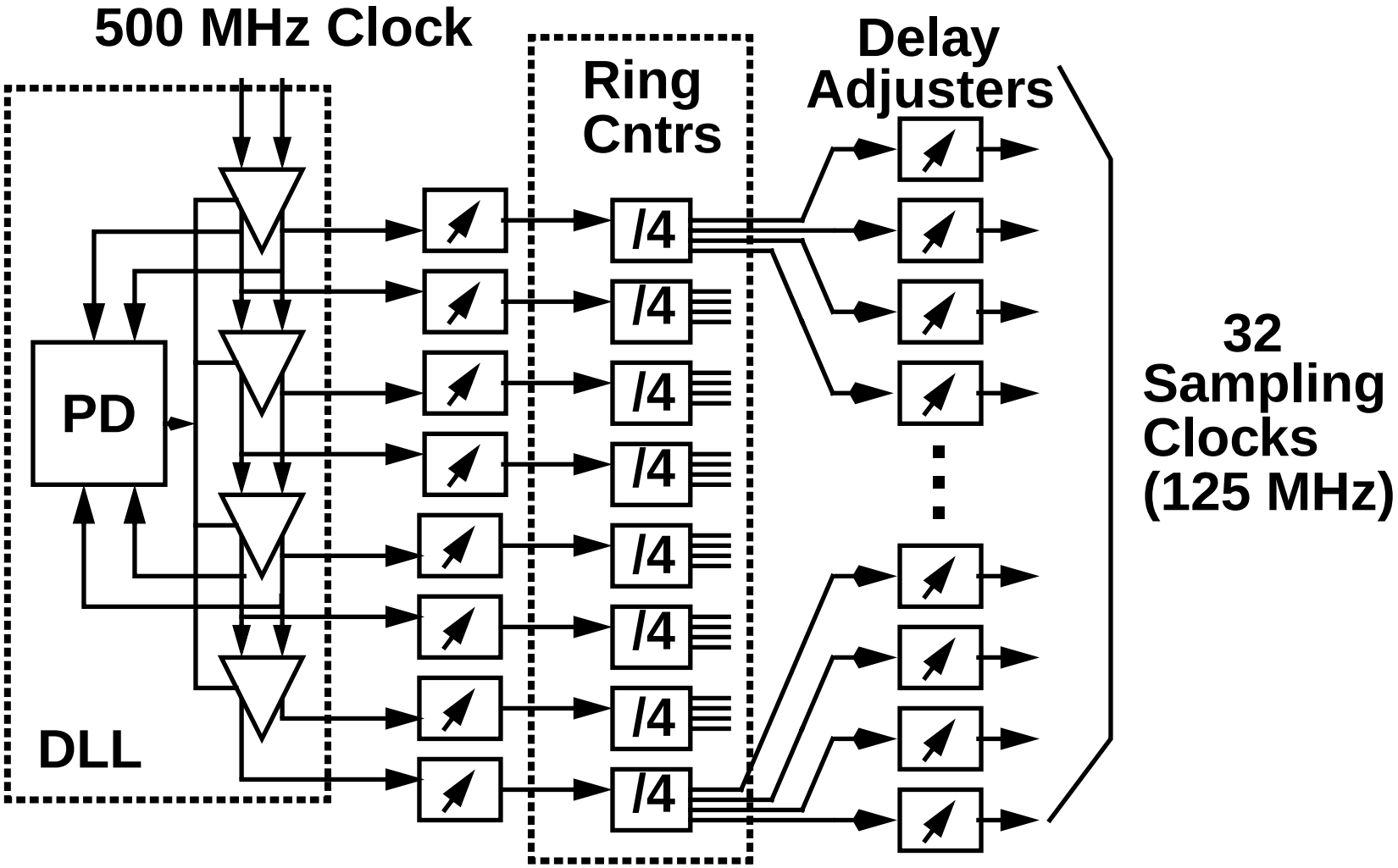
Direct Approach: 31 Stage DLL



- Static timing errors: Error ~ total delay
- Supply noise coupling: Error ~ total delay
- Thermal jitter: Power ~ (total delay)^2

DLL meeting jitter spec would consume entire ADC power budget !!

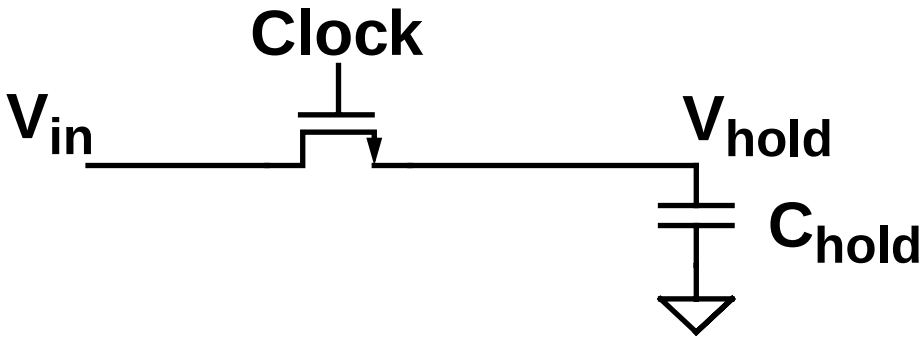
Timing Generator



- Max input edge to sampling edge delay: 2 ns

~ 1 ps jitter **< 1 ps static error after cal**

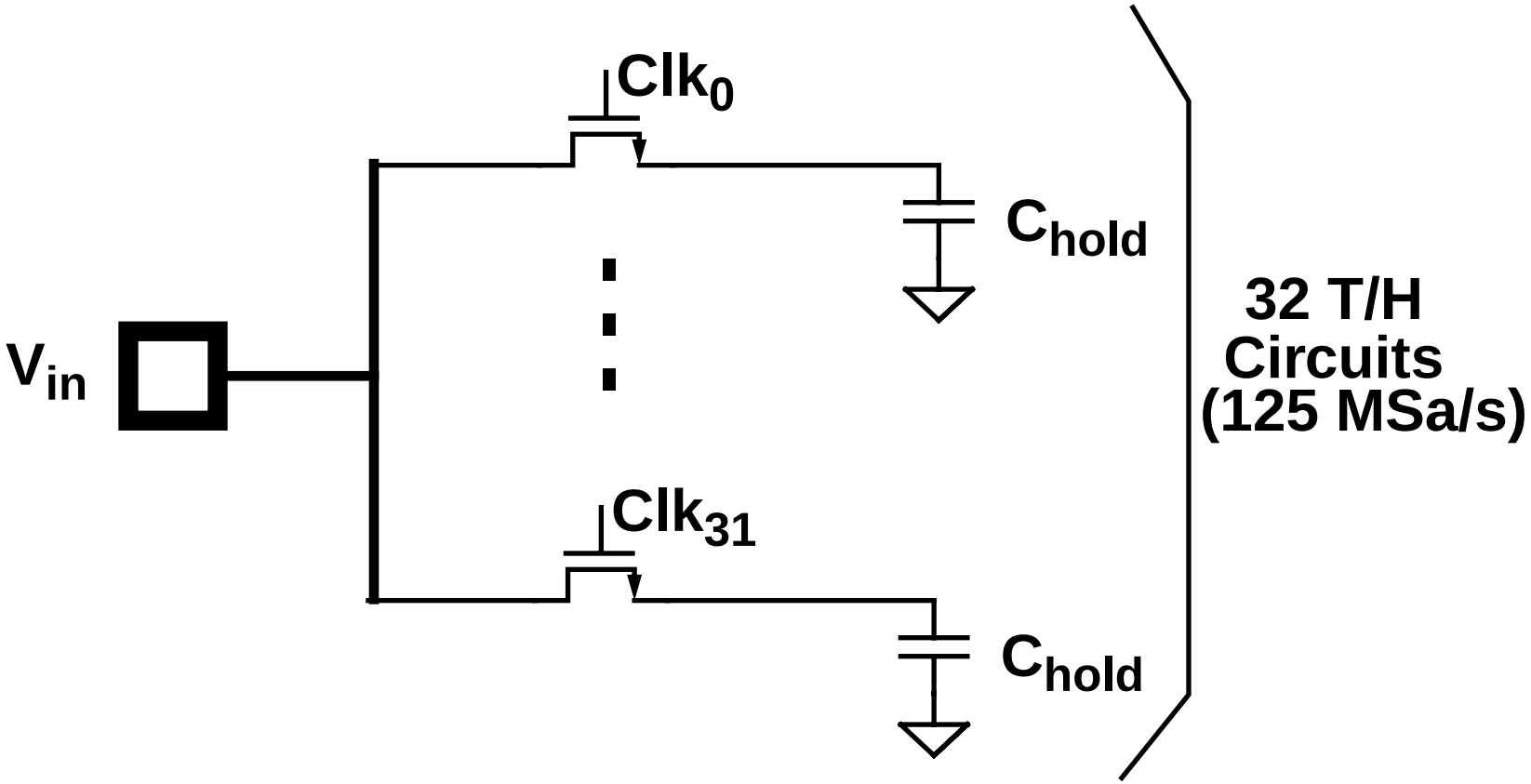
Simplified Input Track/Hold



- To achieve highest bandwidth and linearity:
  - ***ONLY*** 1 NMOS FET in signal path
  - Restrict C_{hold} to only T/H and load parasitics
  - Low common mode input voltage
  - Low-swing differential signal (250 mV peak)
  - Fastest possible full-swing clock edge

2 GHz bandwidth, -50 dB HD3 at 1 GHz

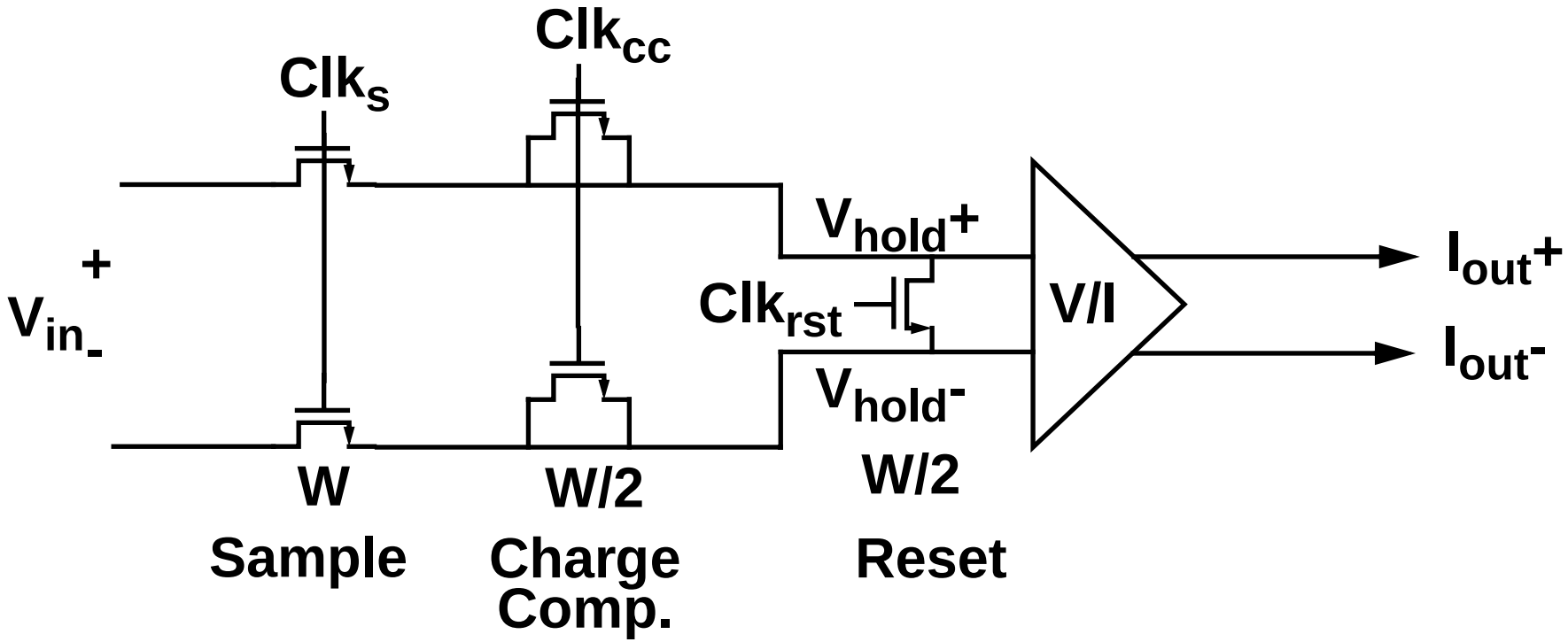
Interleaved Track/Hold Input Circuits



Requirements

- 2 GHz input bandwidth to C_{hold}
- Low parasitics on V_{in}
- Kickback to V_{in} must be independent of signal

Analog Front End Implementation



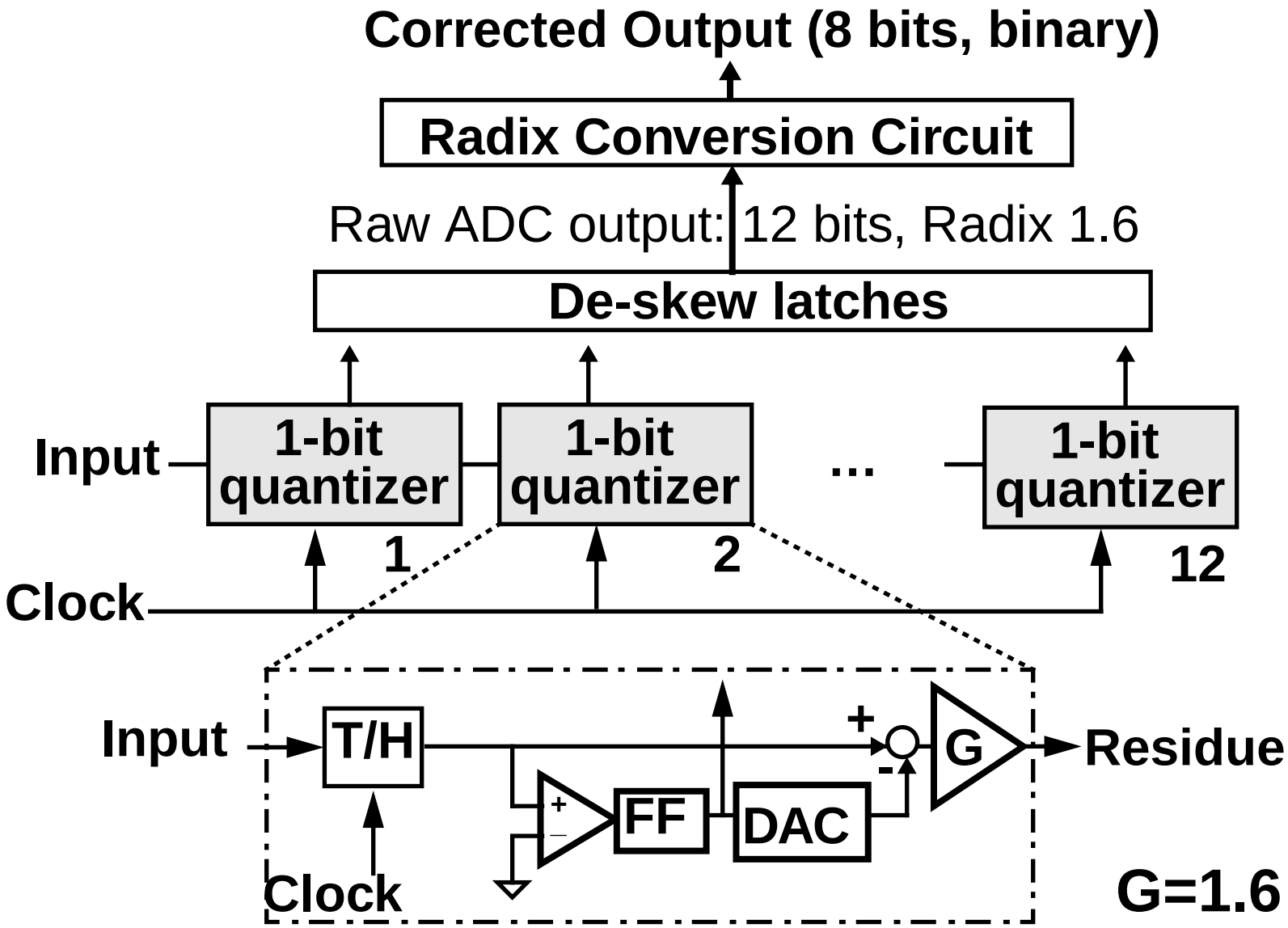
- Parasitic-only hold capacitance (140 fF)
- Only 1 ns pulse width for Clk_s
- Reset phase
- Transconductor (V/I) current output drives ADC

125 MSa/Sec 8-bit Full Nyquist ADC

Key Attribute	Reason
Pipelined Architecture	Low power Small area Low input capacitance
1 bit / Stage	Highest speed pipeline
Open-loop amplifiers Current mode signals (Switched current mirrors)	Fastest settling No explicit capacitors Small Area
Scale for thermal noise	Smallest area and power

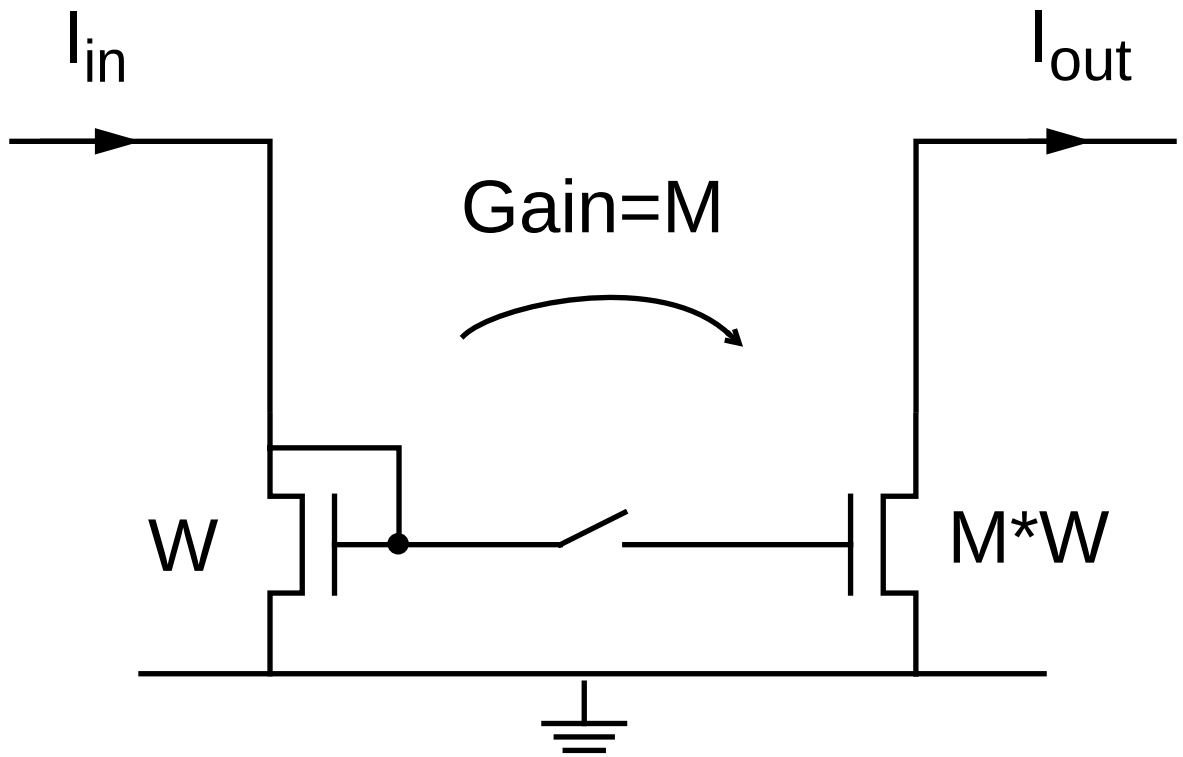
Making it work	
Reduce Radix to 1.6	Achieves Redundancy
Digital Calibration	Corrects amplifier gain and offset errors.

Pipeline ADC Block Diagram



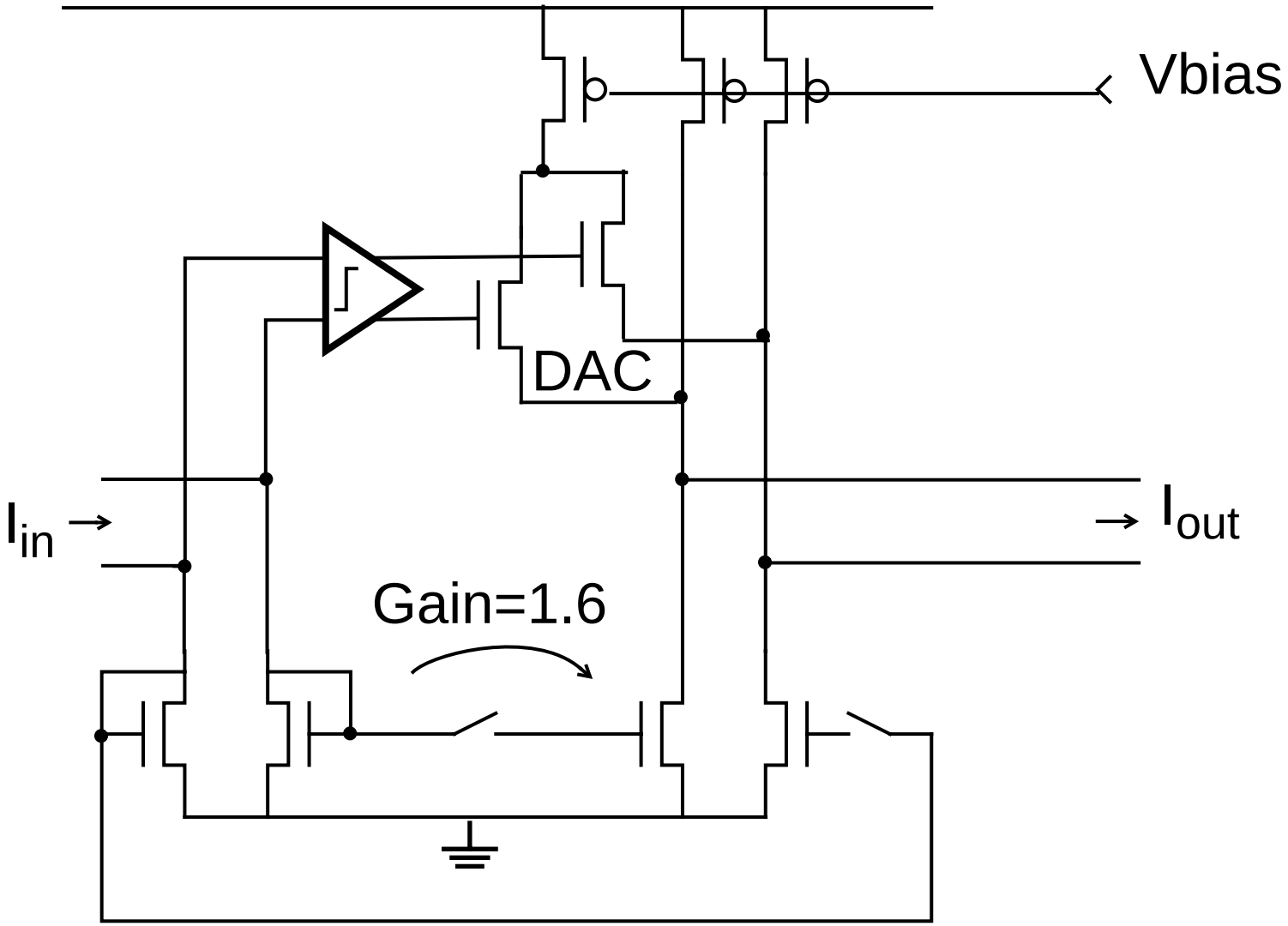
- Only 1 comparator per stage

Current-Mode T/H and Gain



- Good Linearity: Current mirrors with cascodes are 8 bit linear.
- Poor Accuracy: Gain and offset errors

Current-Mode ADC Stage

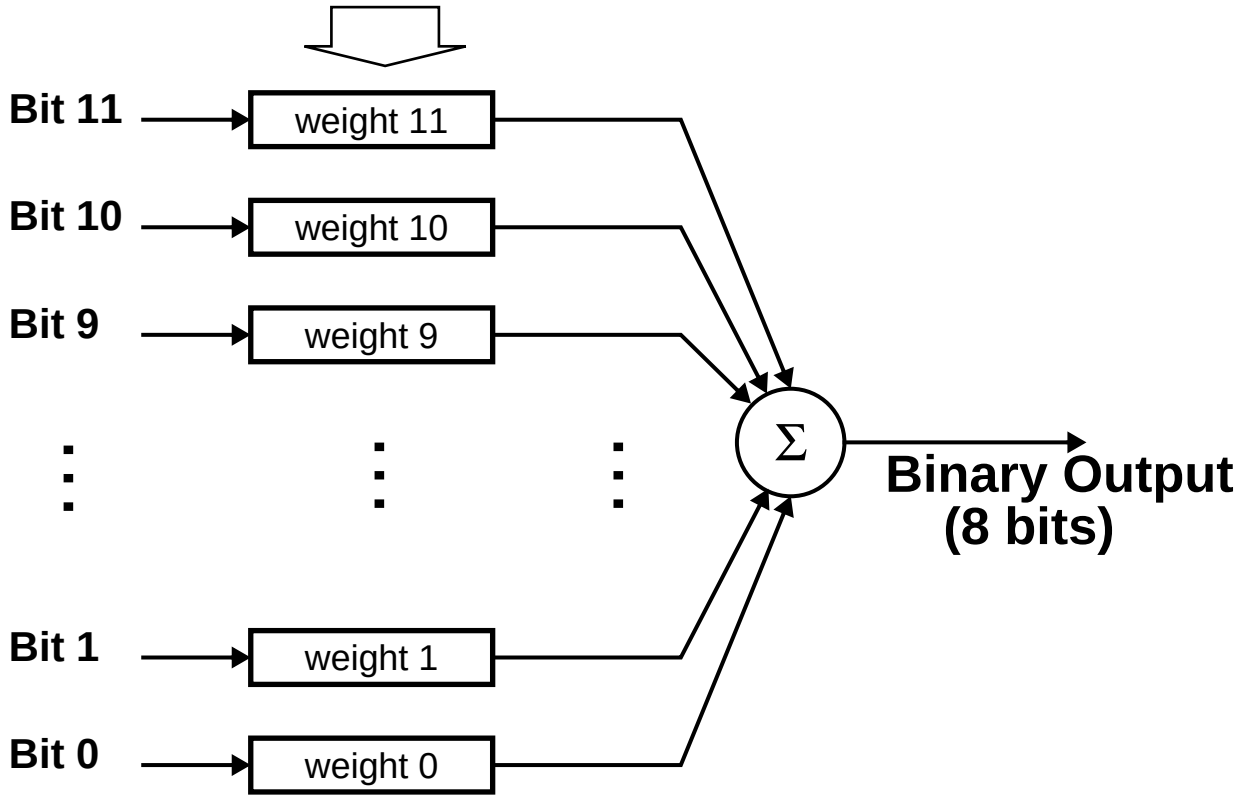


Current-Mode Pipeline ADC

- State of the art speed/power ratio for an 8-bit ADC
  - 125 MSa/s, full nyquist performance
  - 80 mW total
    - 20 mW V/I buffer
    - 40 mW pipeline
    - 20 mW radix converter
- Small Area
  - 0.3 mm^2

Radix Converter - Principle of Operation

Calculate and download bit weights during cal.



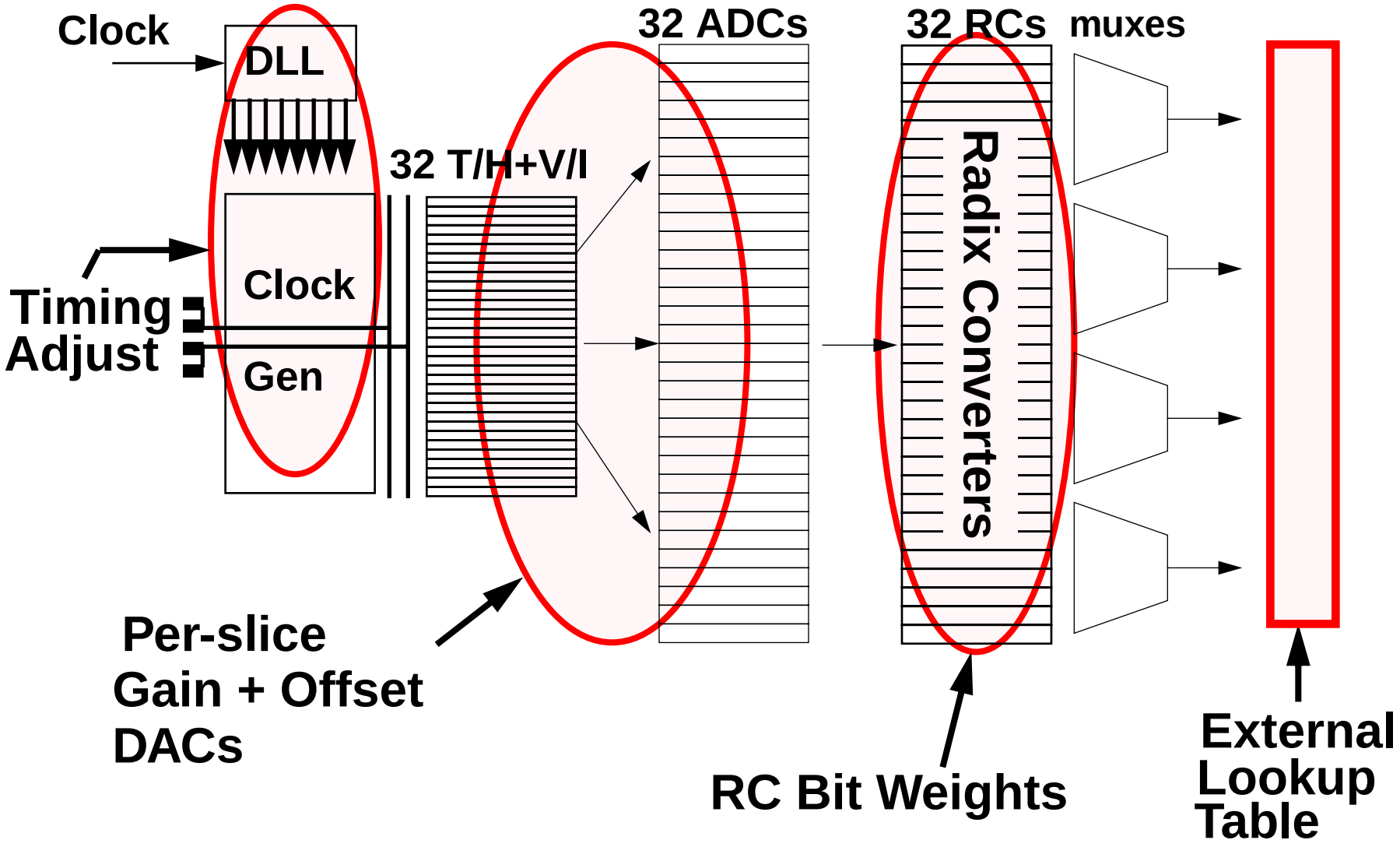
Output = $b_{11}.w_{11} + b_{10}.w_{10} + \ldots + b_1.w_1 + b_0.w_0$

- Look-up table is an alternative.
- This ADC uses a hybrid look-up/adder.

Supply and Substrate Noise Reduction

- Fully differential analog path
- Very low-noise digital logic family (SCL - Source Coupled Logic)
  - Differential Logic
  - Constant Supply Current
  - Generates less noise than the ADC Comparators !!
- Differential output drivers
- Chip-level supply and substrate noise simulation for design verification.

What Needs To Be Calibrated?



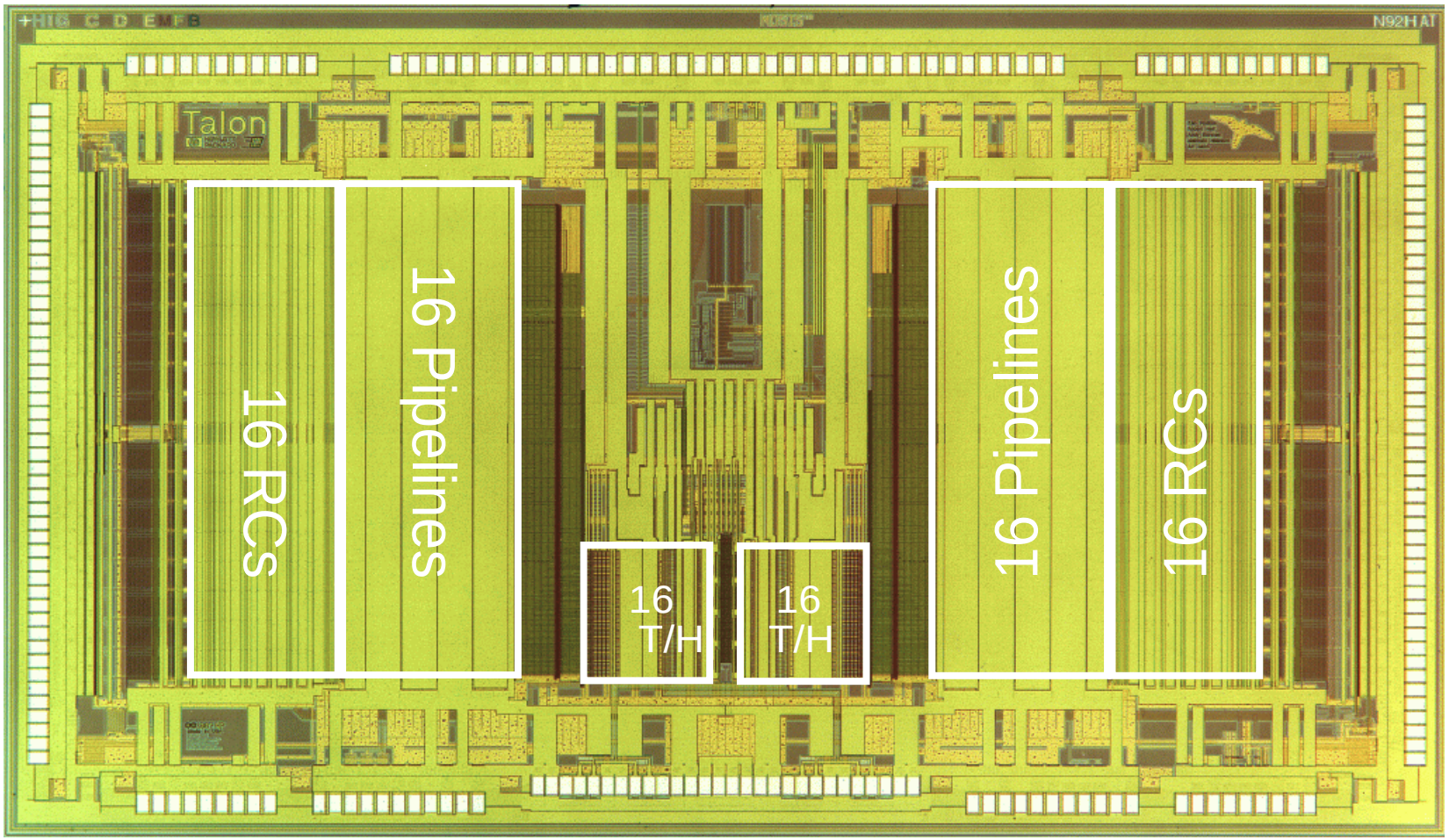
- Offline Calibration with DC and Pulse sources

Offline Calibration

- DC Linearity Calibration
  - Use a DC ramp input, observe ADC radix bits
  - Analog gain and offset trim per path
  - Use least squares fit on a large record to find optimal bit weights and 3rd harmonic fit.
  - Least squares fit minimizes INL
- Timing Calibration
  - Apply a pulse train with fast edges
  - Use an FFT to measure phase delay on each T/H
  - Adjust time delays, and iterate

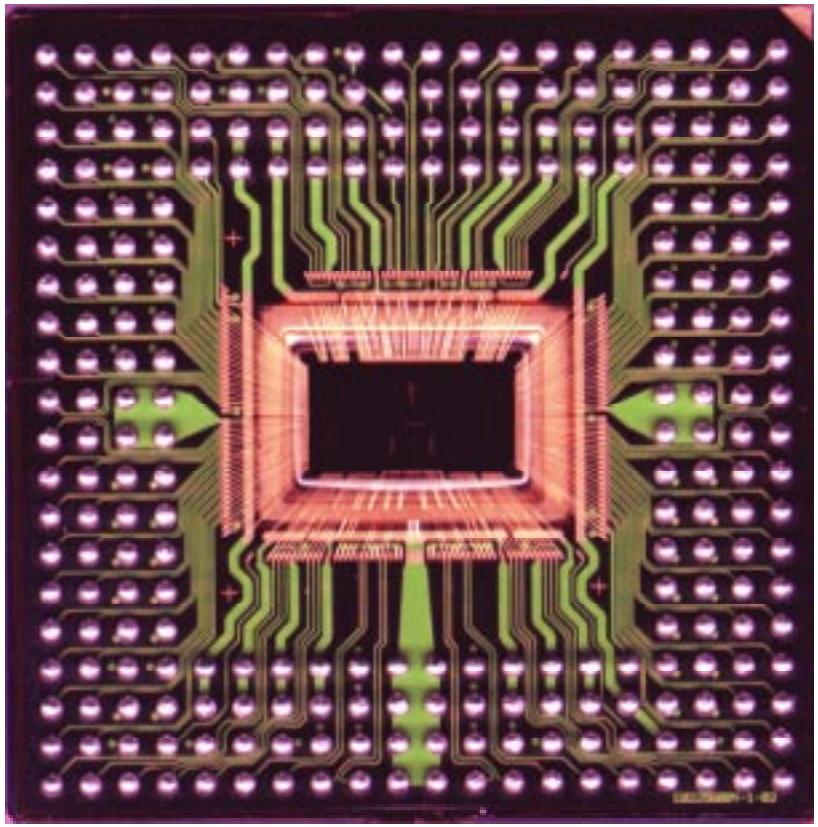
Full ADC calibration takes about 3 minutes

ADC Chip Layout



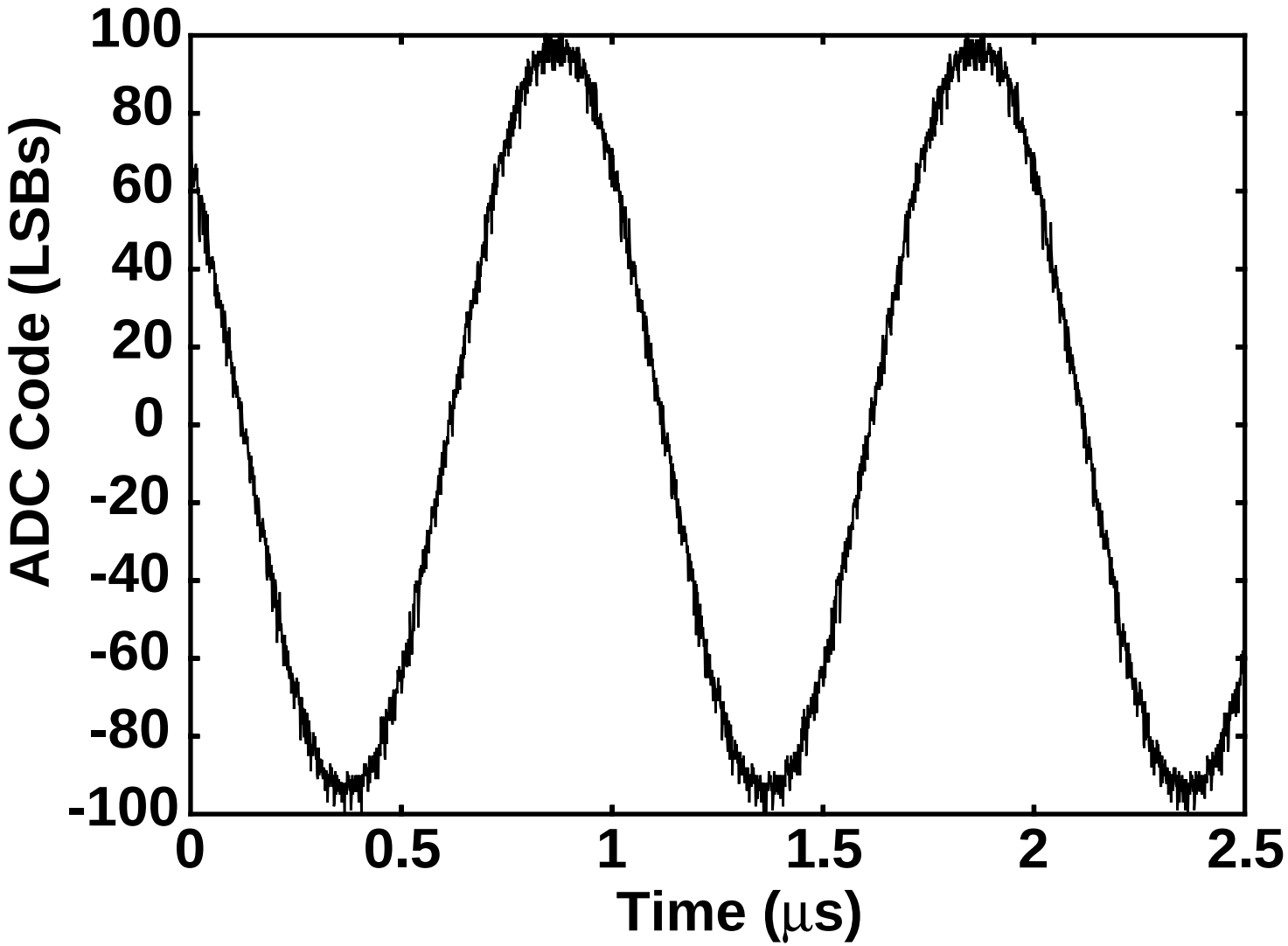
7.1 mm x 4.0 mm **300,000 FETs** **4.6 W**

ADC 256-Ball TBGA Package



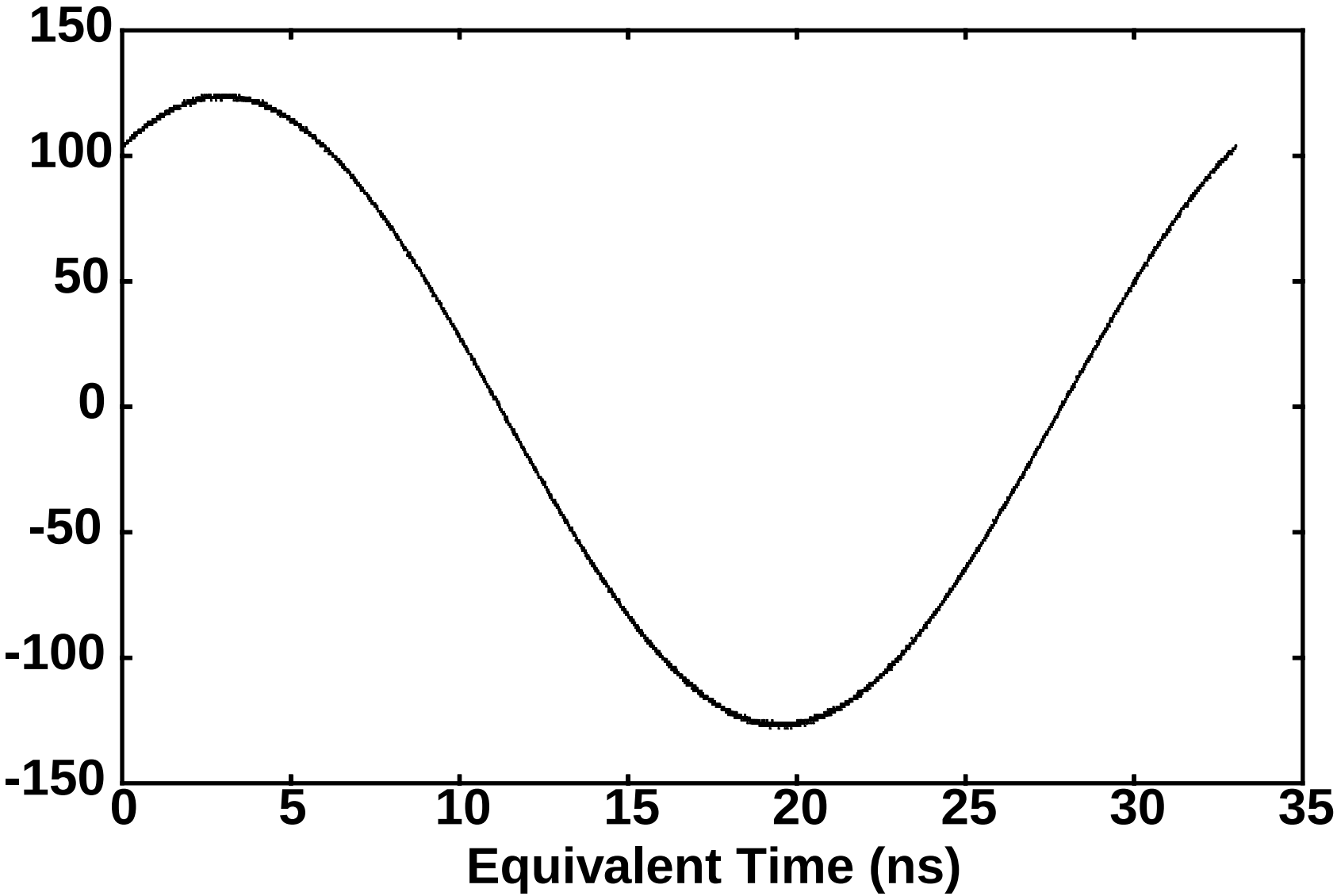
- Copper body
- Controlled-impedance lines
- Custom layout, standard ball pattern

Acquisition Before Calibration



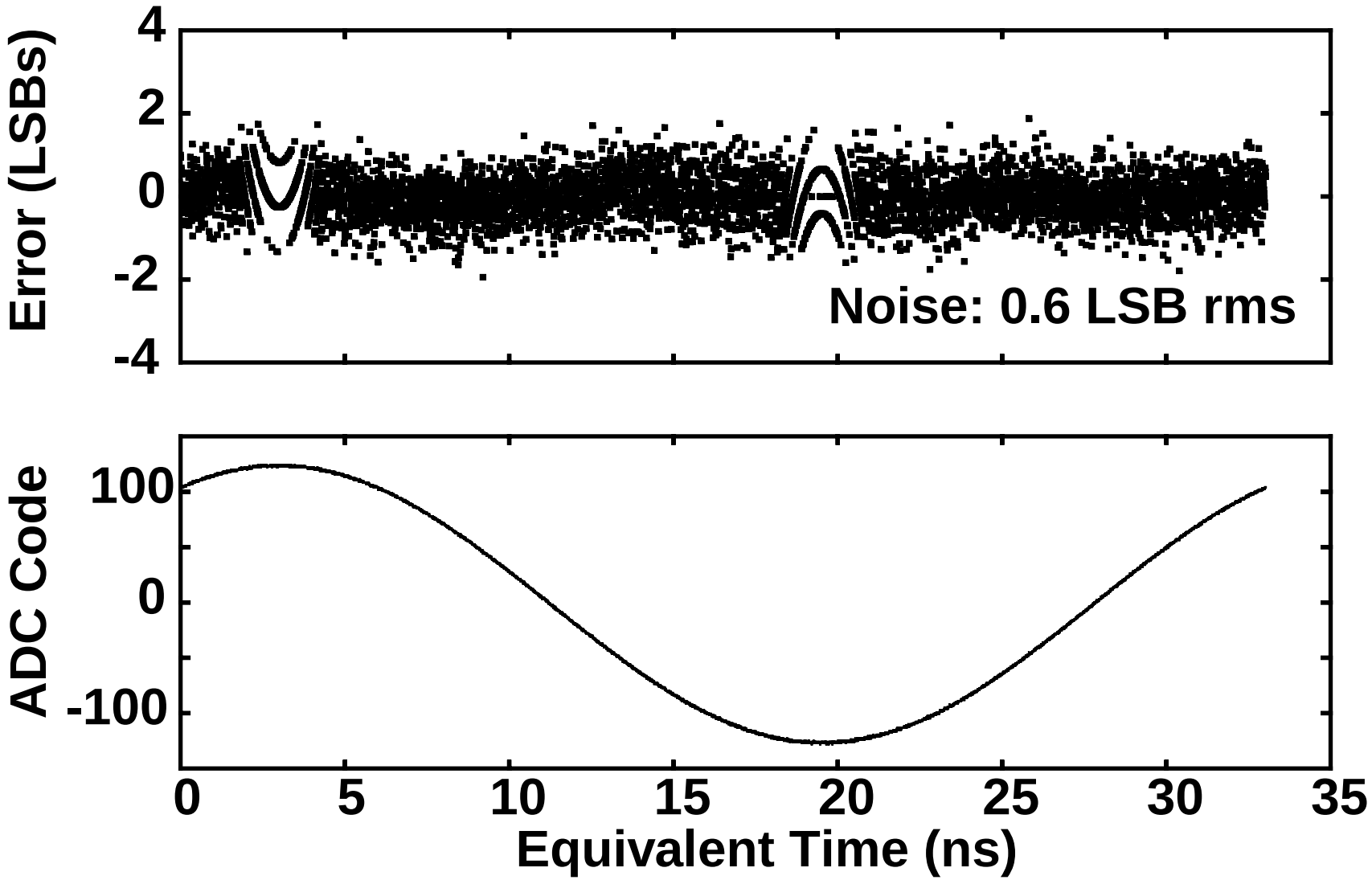
~ 5 effective bits

Acquisition With Calibration



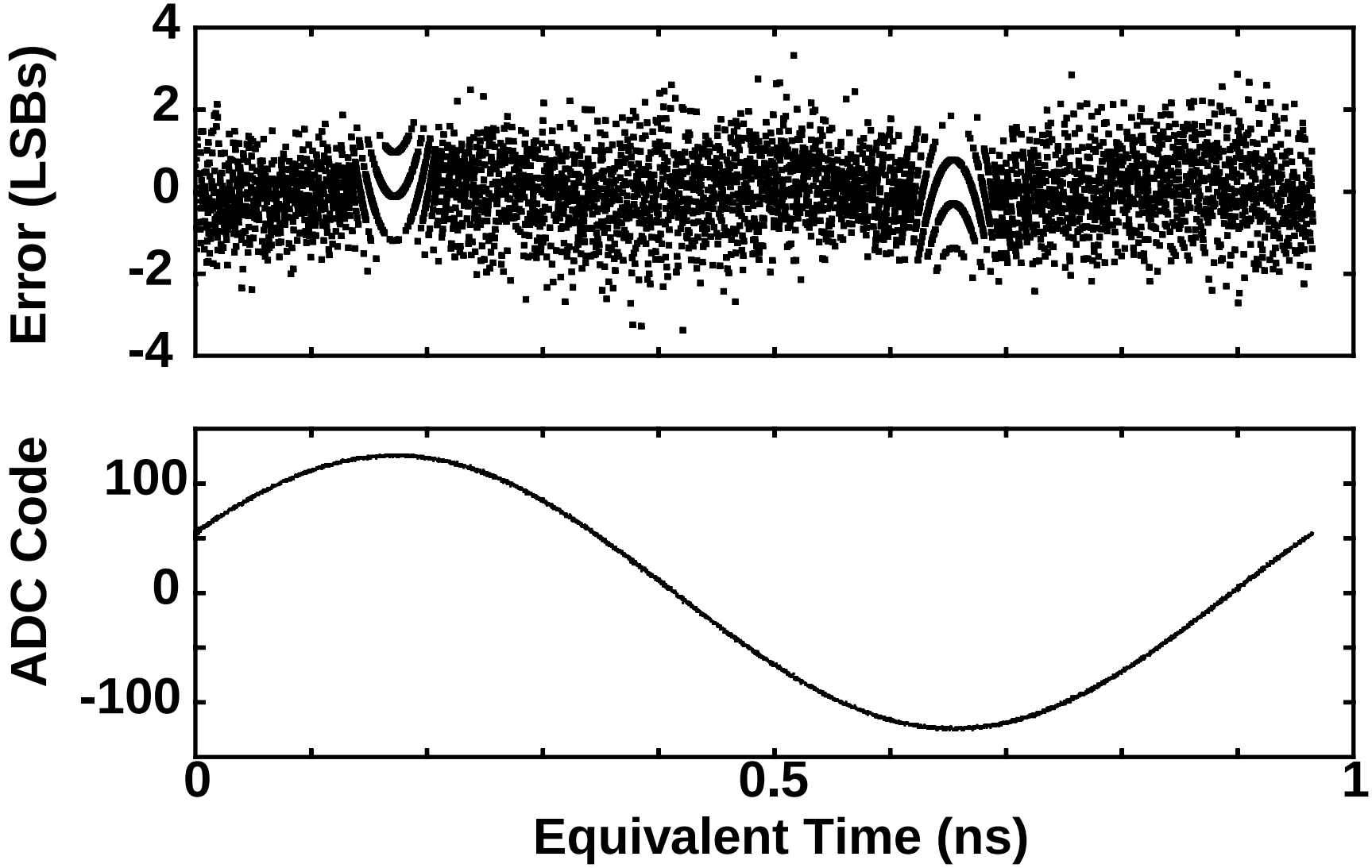
F_s=4000 MSa/sec F_{in}=30.27 MHz 7.0 effective bits

Acquisition With Calibration



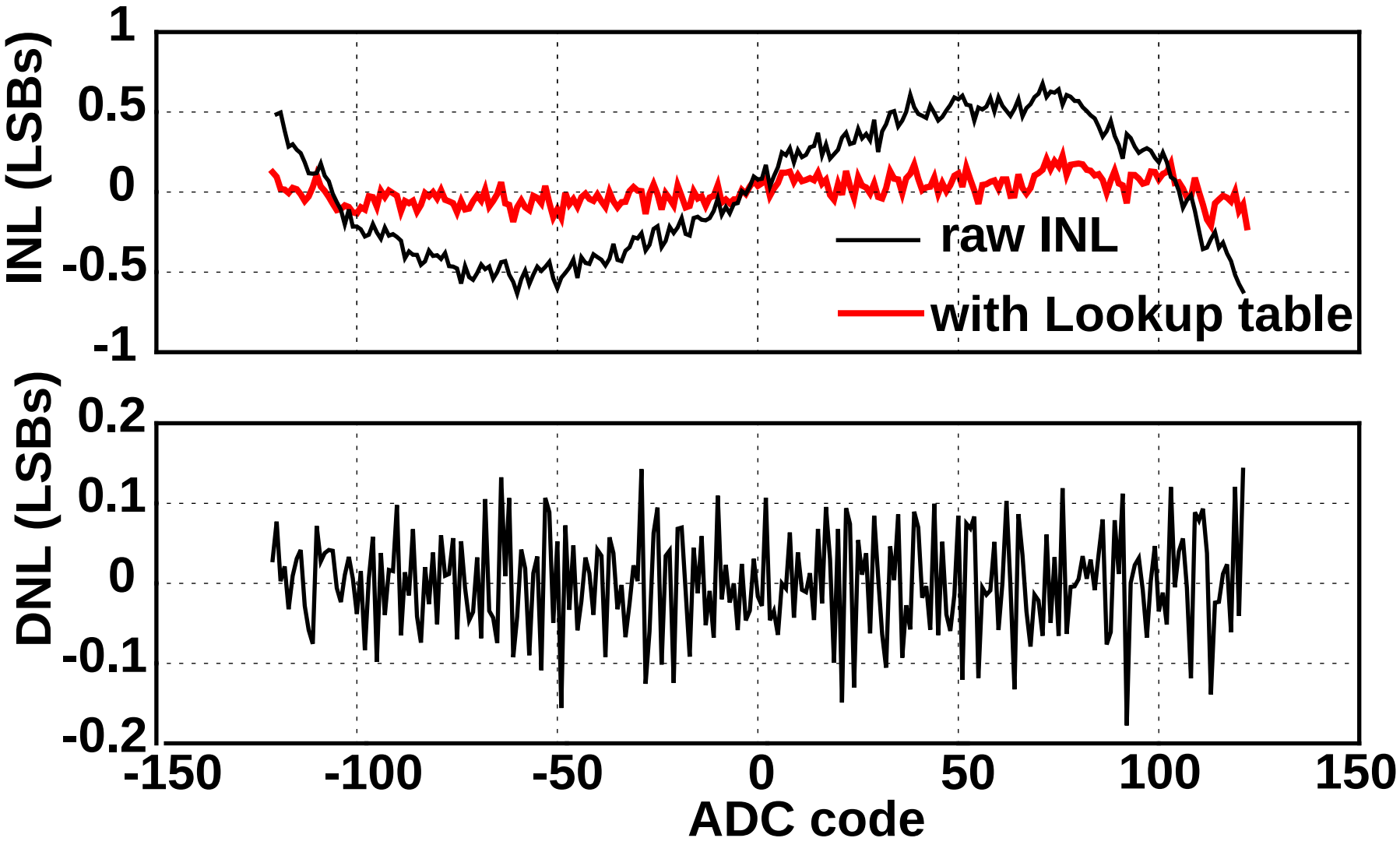
F_s=4000 MSa/sec F_{in}=30.27 MHz 7.0 effective bits

Full Calibration, With 1 GHz Input

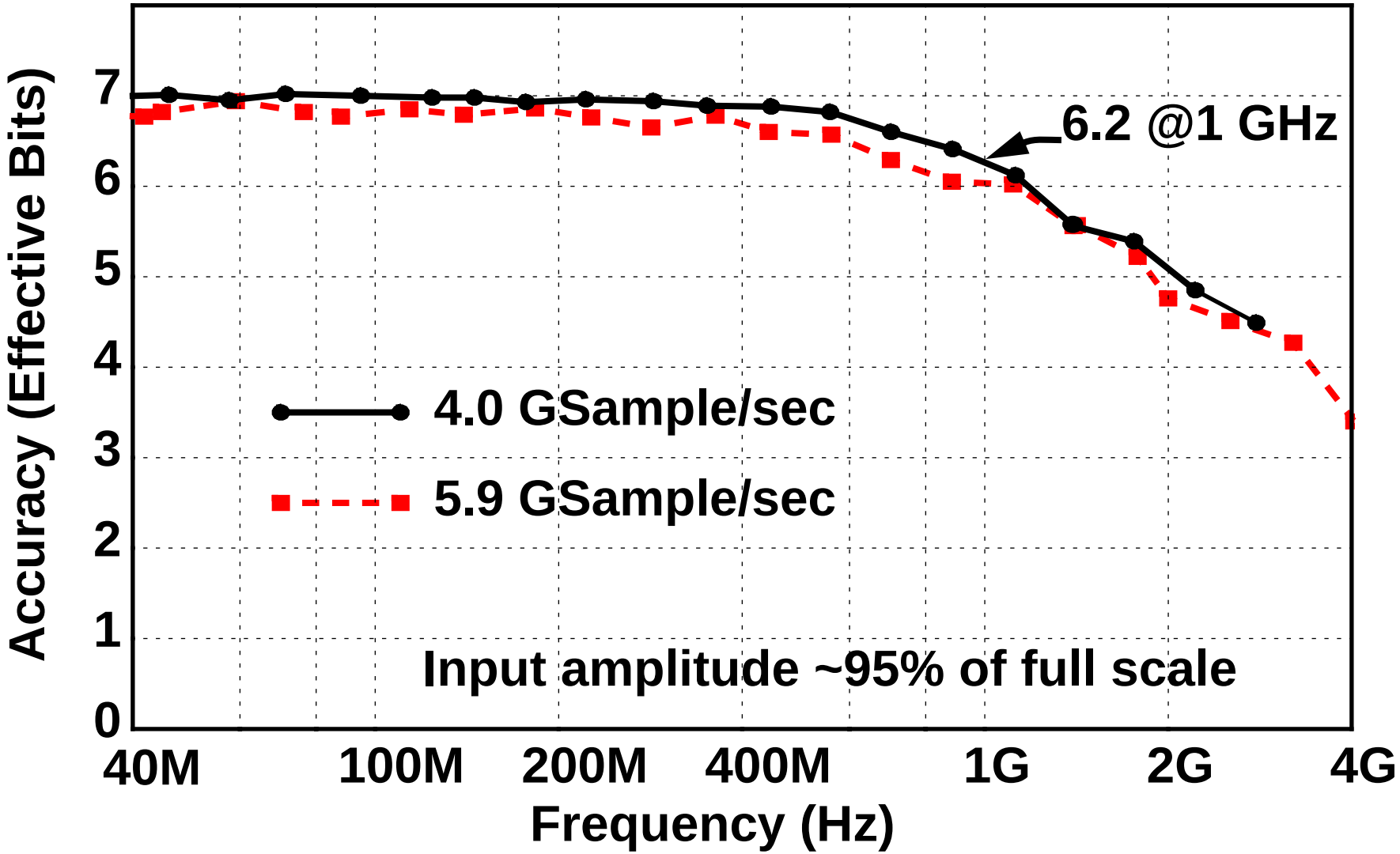


F_s=4000 MSa/s F_{in}=1026.4 MHz 6.35 effective bits

Static Linearity

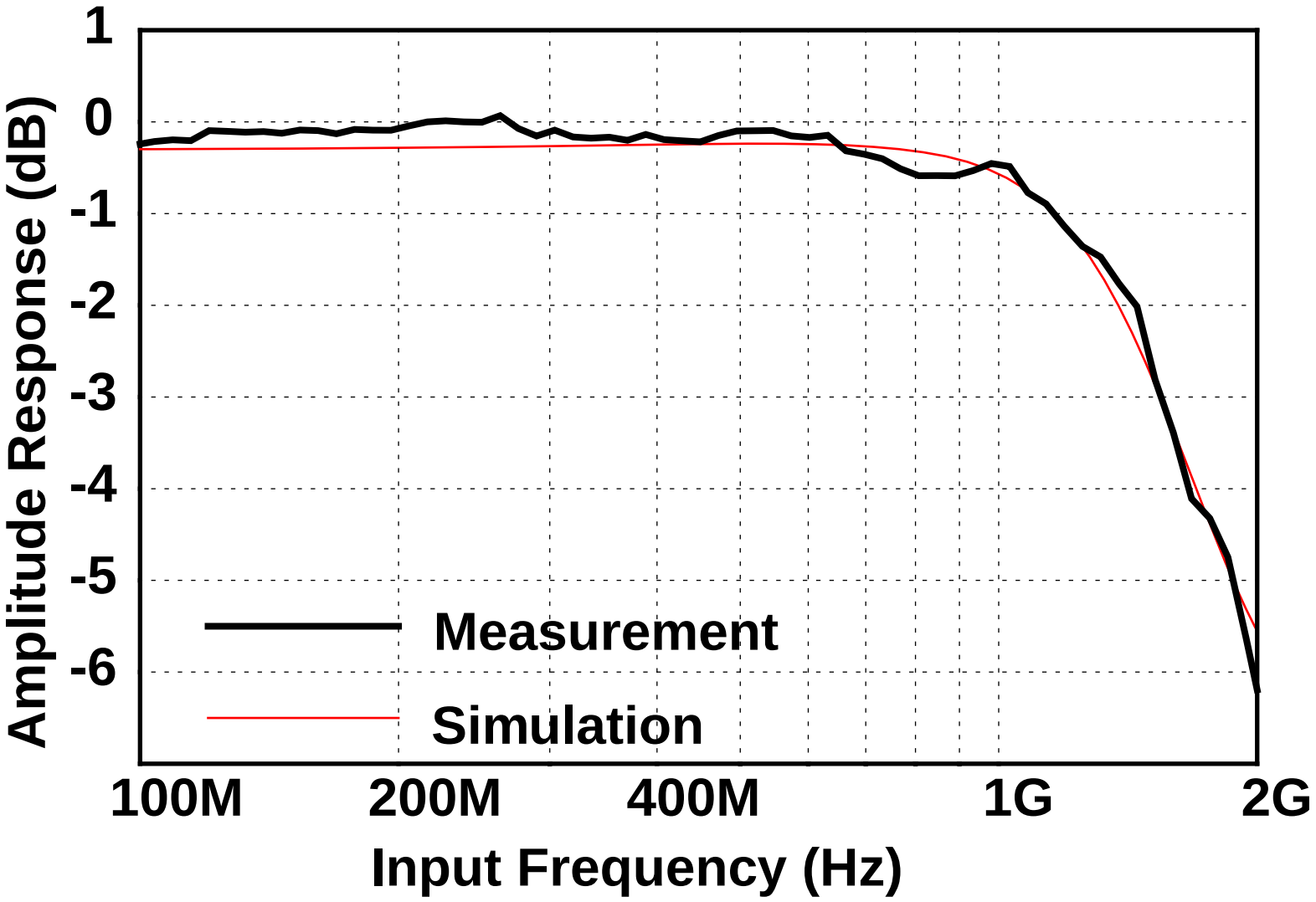


ADC Effective Bits vs Input Frequency



1.2 ps rms clock error

ADC Amplitude Response

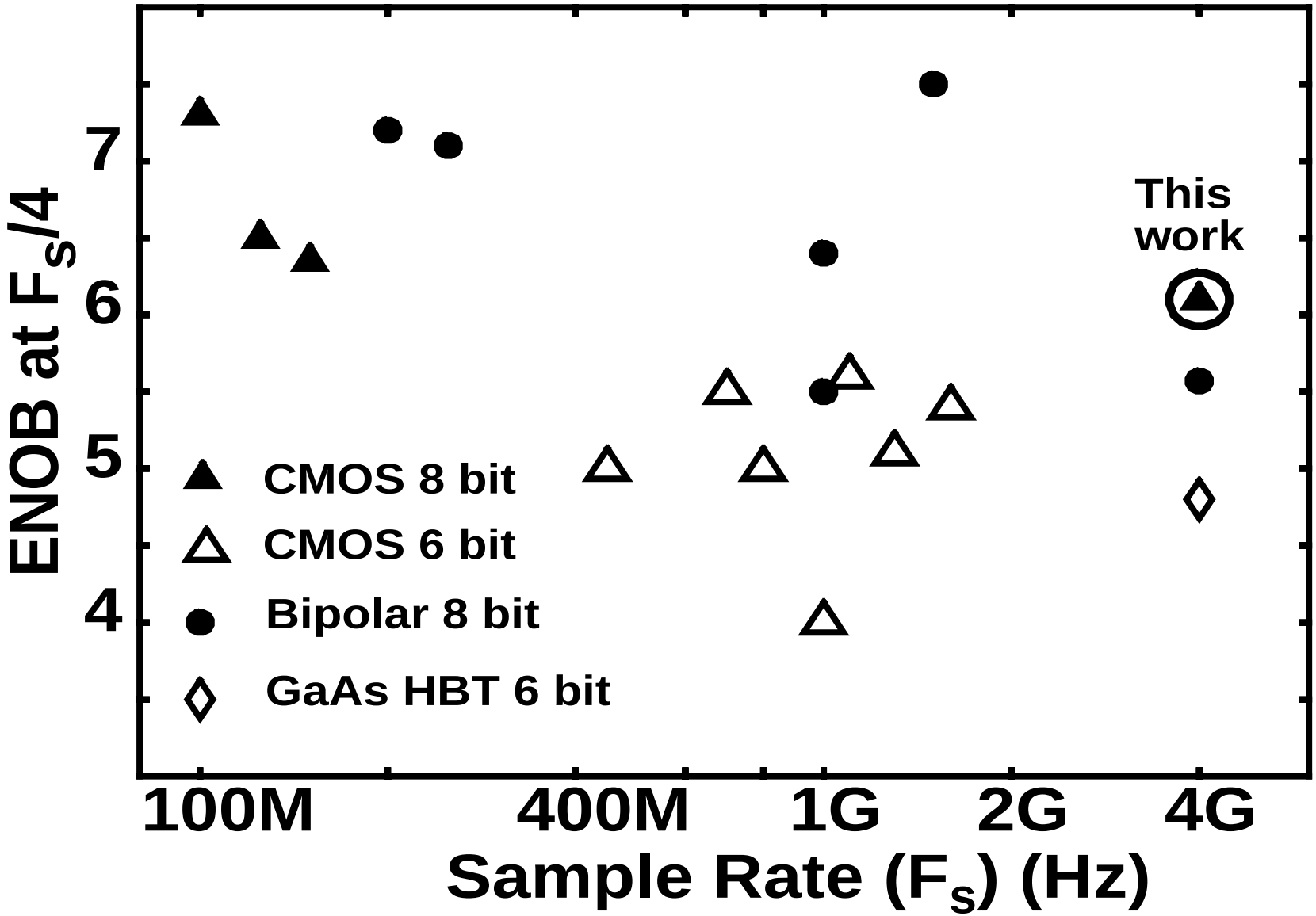


-1 dB at 1.3 GHz -3 dB at 1.6 GHz

ADC Chip - Key Specs

	Measured	Units
Nominal Sample Rate	4	GSa/s
Sample Rate Range	0.1 - 5.9	GSa/s
Resolution	8	bits
3 dB Bandwidth	1.6	GHz
Accuracy 30 MHz 1 GHz	 7.0 6.2	 effective bits (ENOB)
Noise	0.6	LSB rms
INL / DNL	$\pm$0.3 / $\pm$0.2	LSB
Power	4.6 W at 3.3 V	
IC Technology	0.35 μm CMOS	
Chip Size	7.14 x 4.04 mm^2	
Transistors	300,000	
Package	256 ball TBGA	

Monolithic ADCs



Summary

- Features:
  - Interleaving of 32 ADCs
  - Precision timing generator for 32 clock phases
  - Current-mode pipeline provides a superior speed/ power ratio
  - Extensive calibration to achieve accuracy
- Results:
  - 2x lower power/Gsample than any reported GSa/s 8-bit ADC
  - Highest reported clock rate for 6-8 bit CMOS ADCs
  - Highest reported accuracy at 4 GSa/s